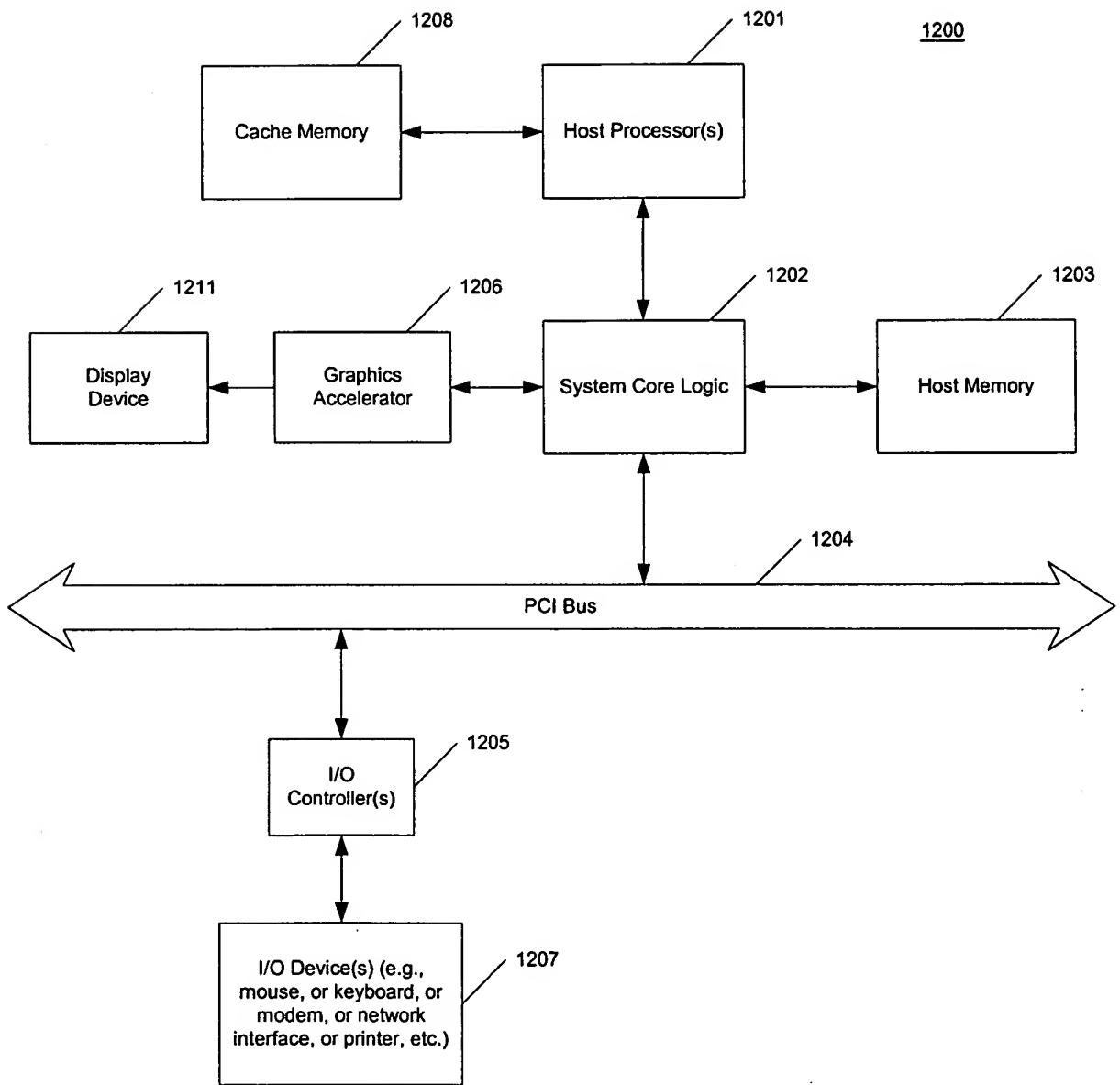


**Figure 1**



**Figure 2**

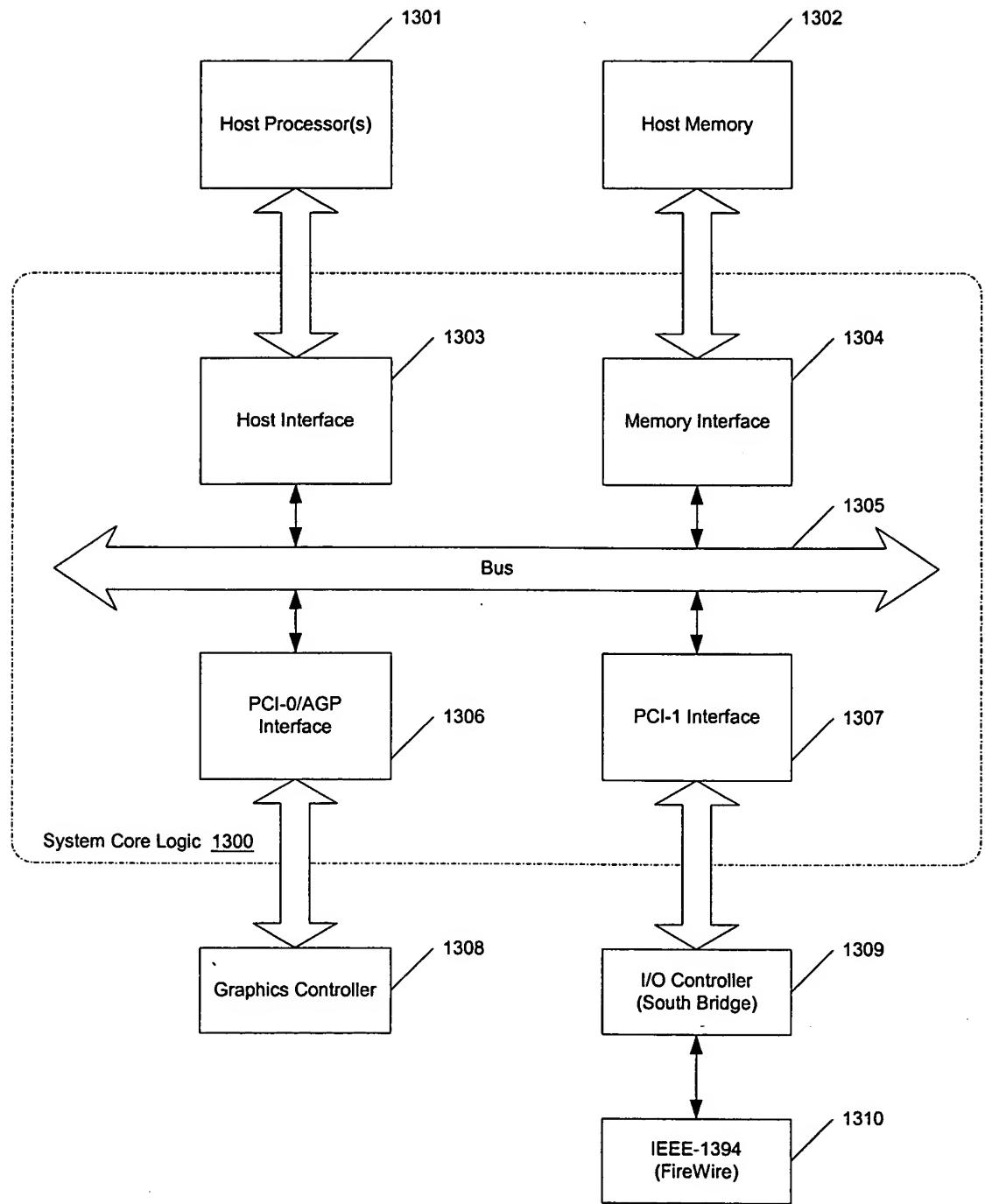
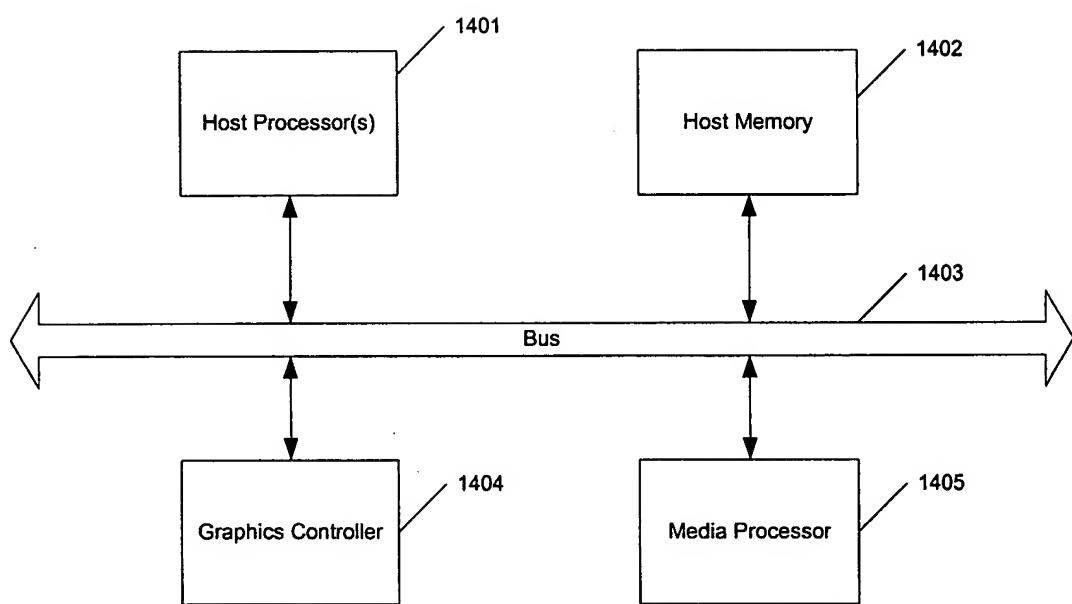
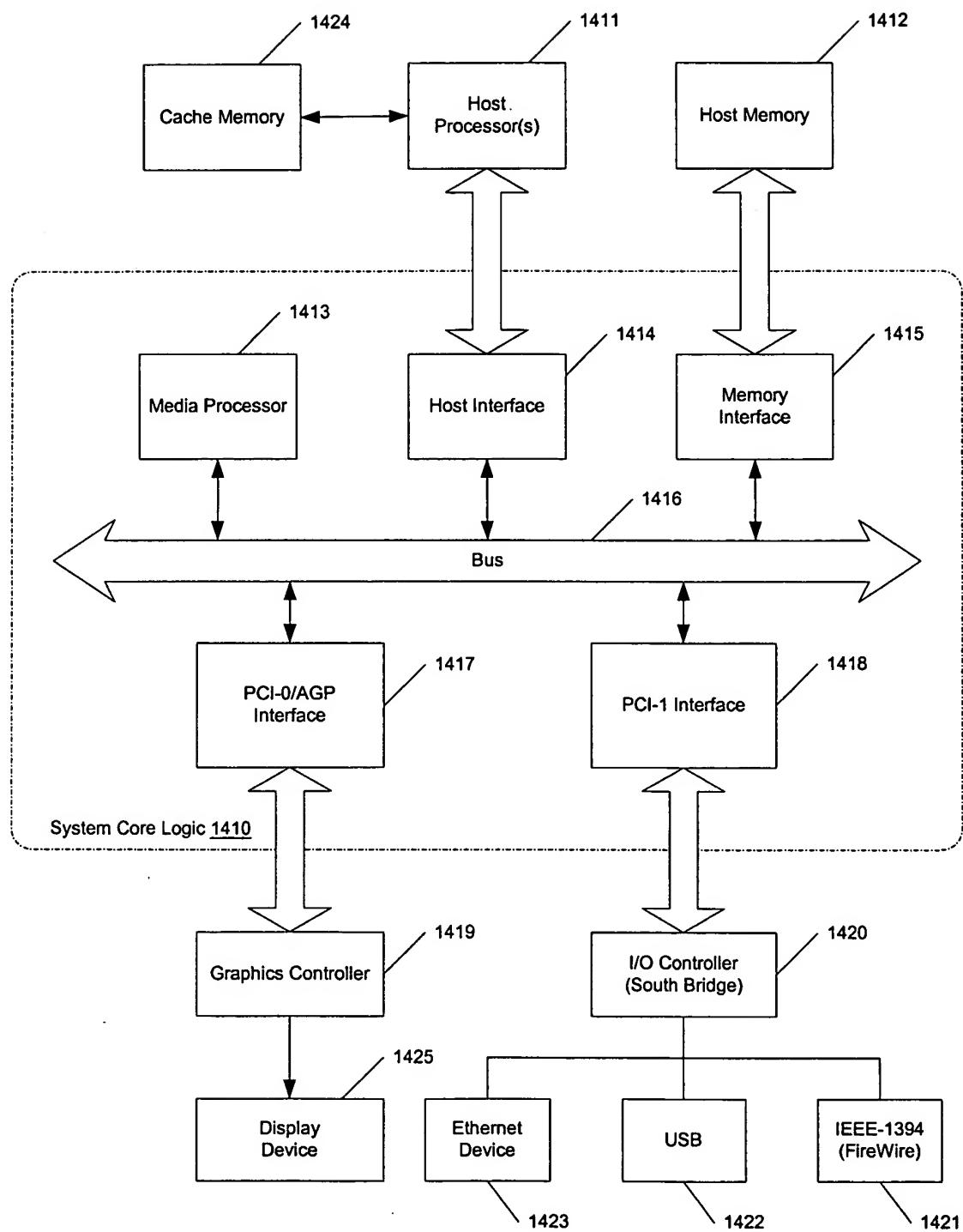


Figure 3

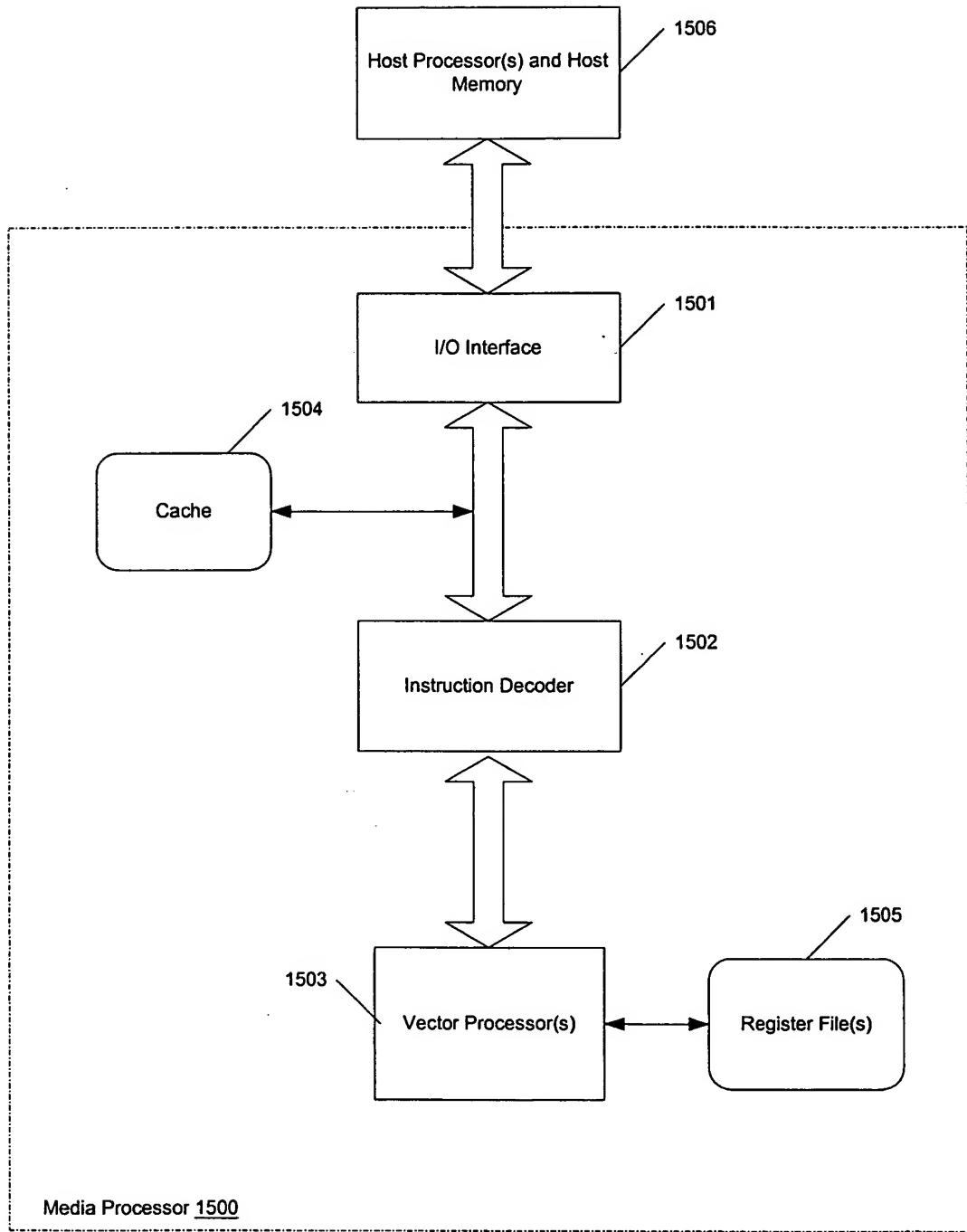
1400



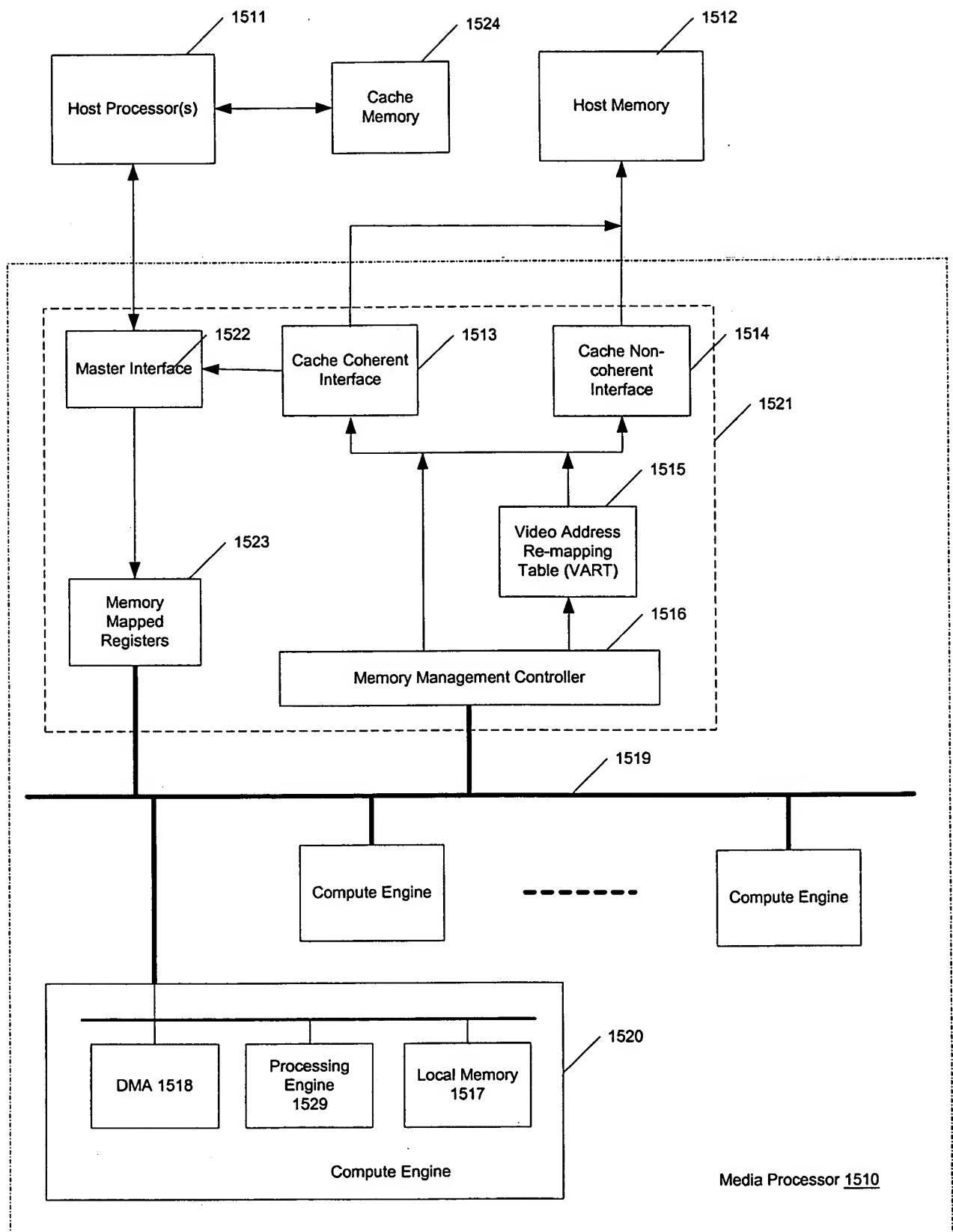
**Figure 4A**



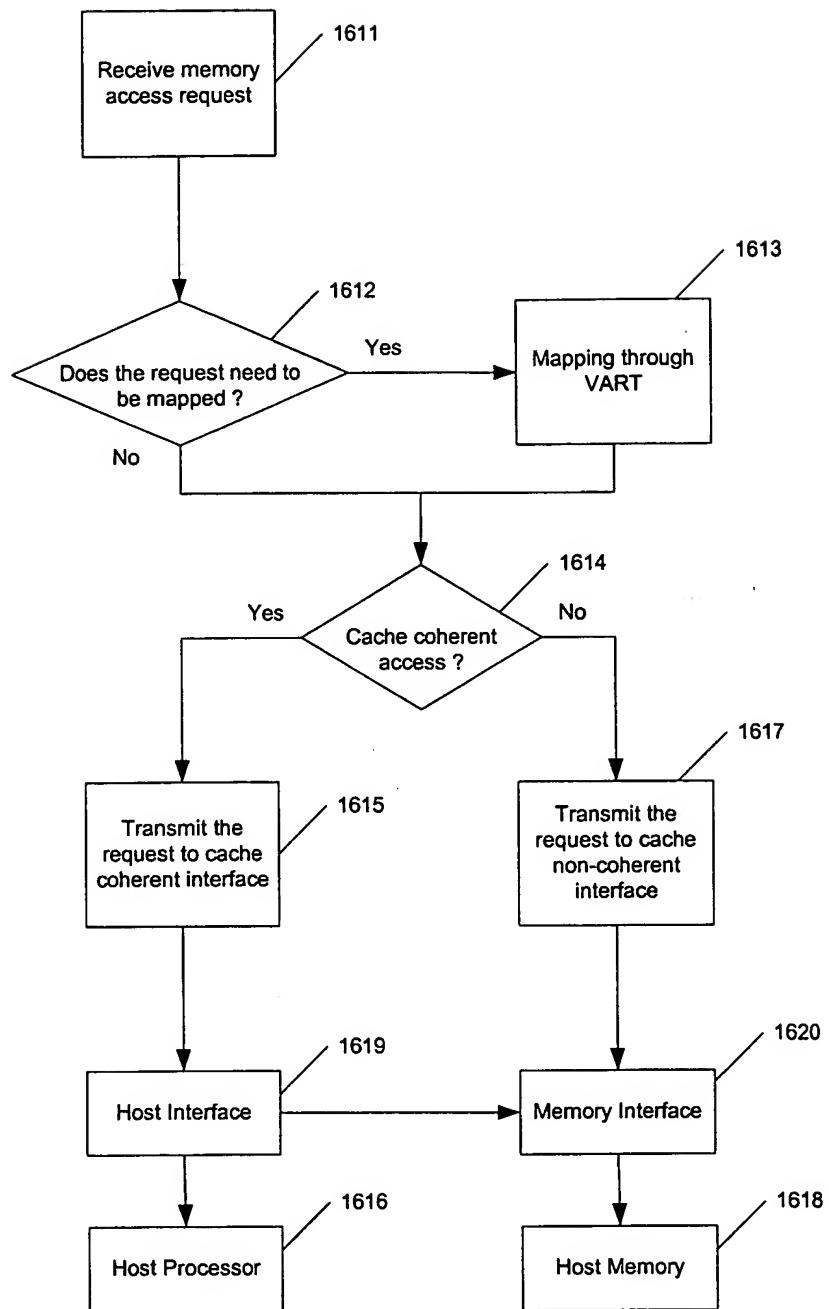
**Figure 4B**



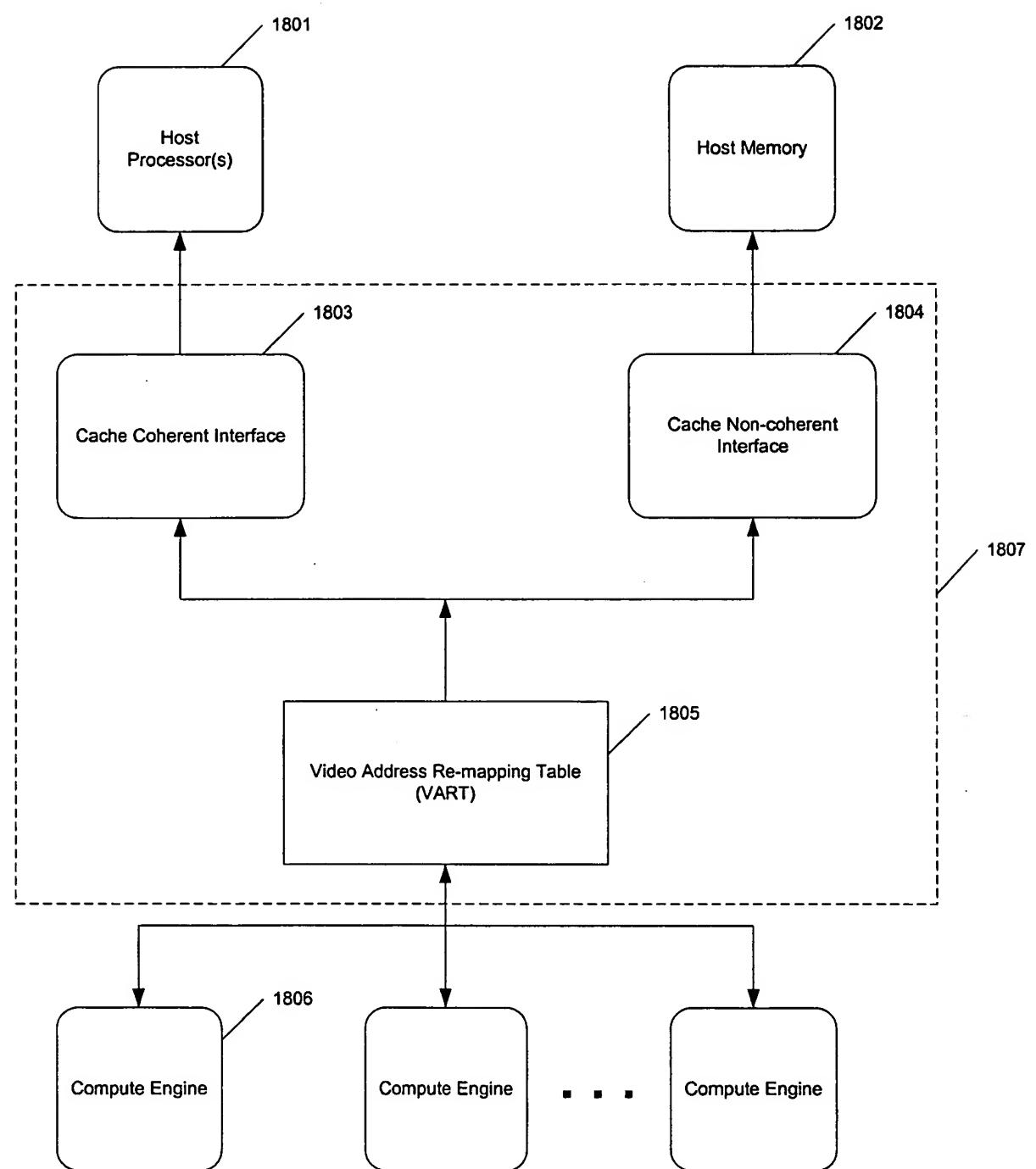
**Figure 5A**



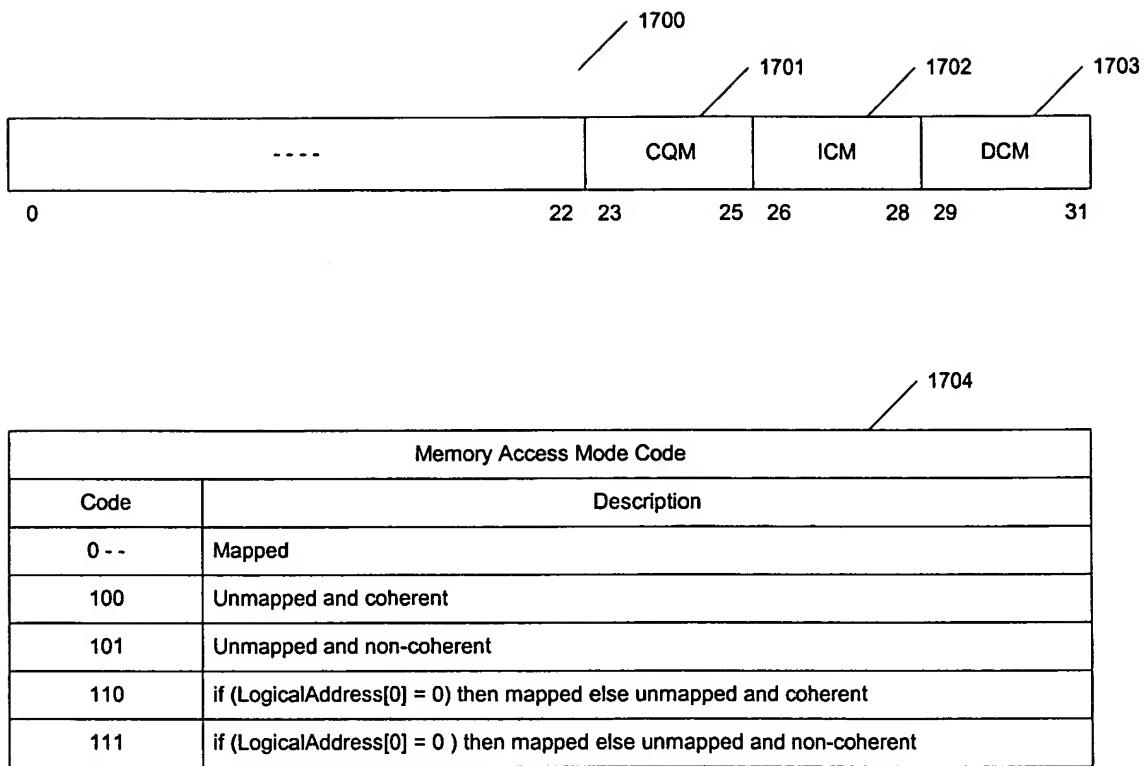
**Figure 5B**



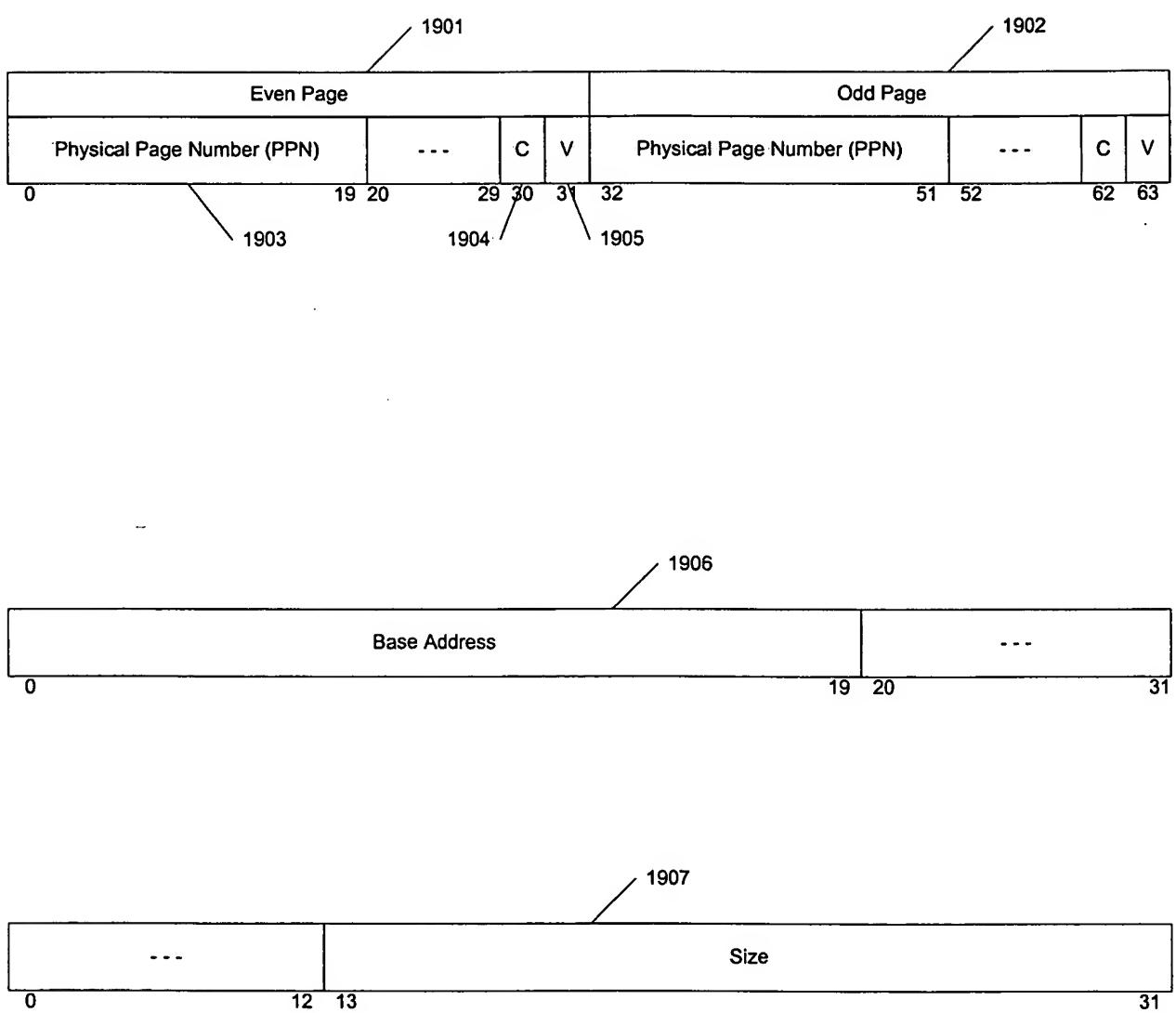
**Figure 6**



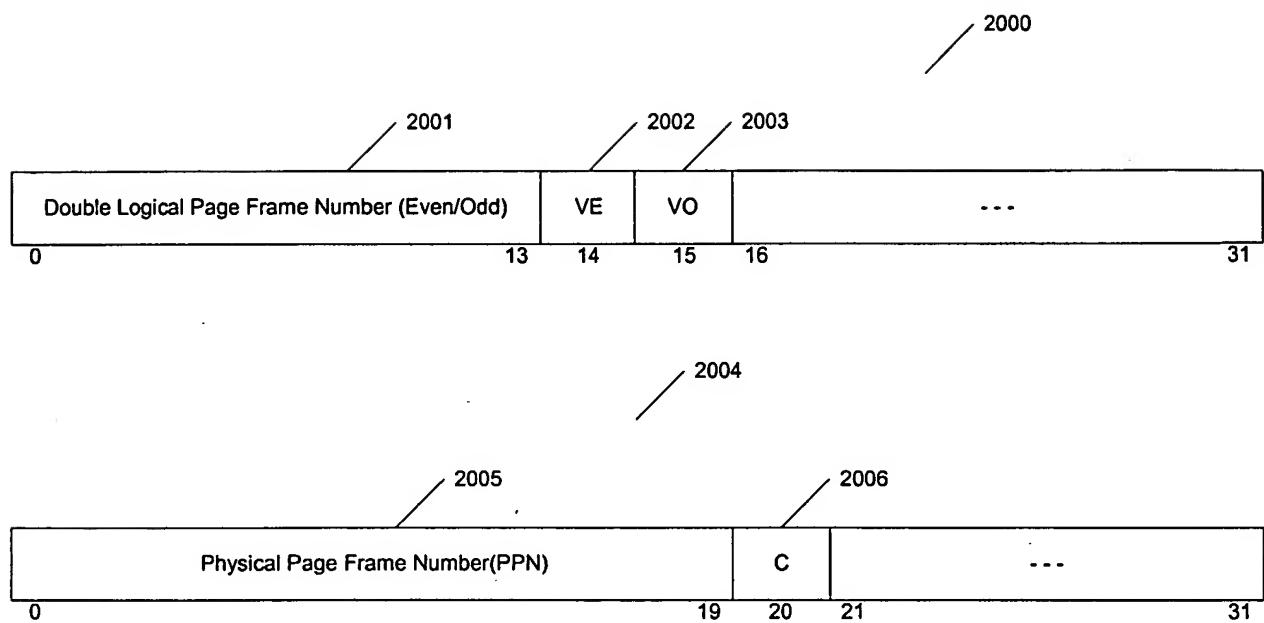
**Figure 8**



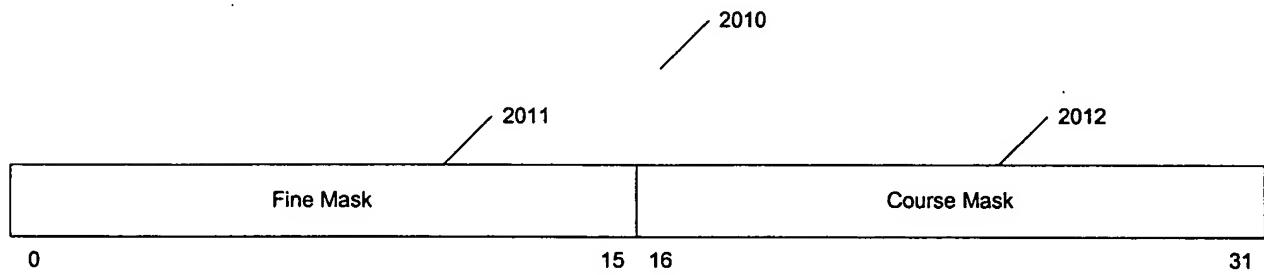
**Figure 7**



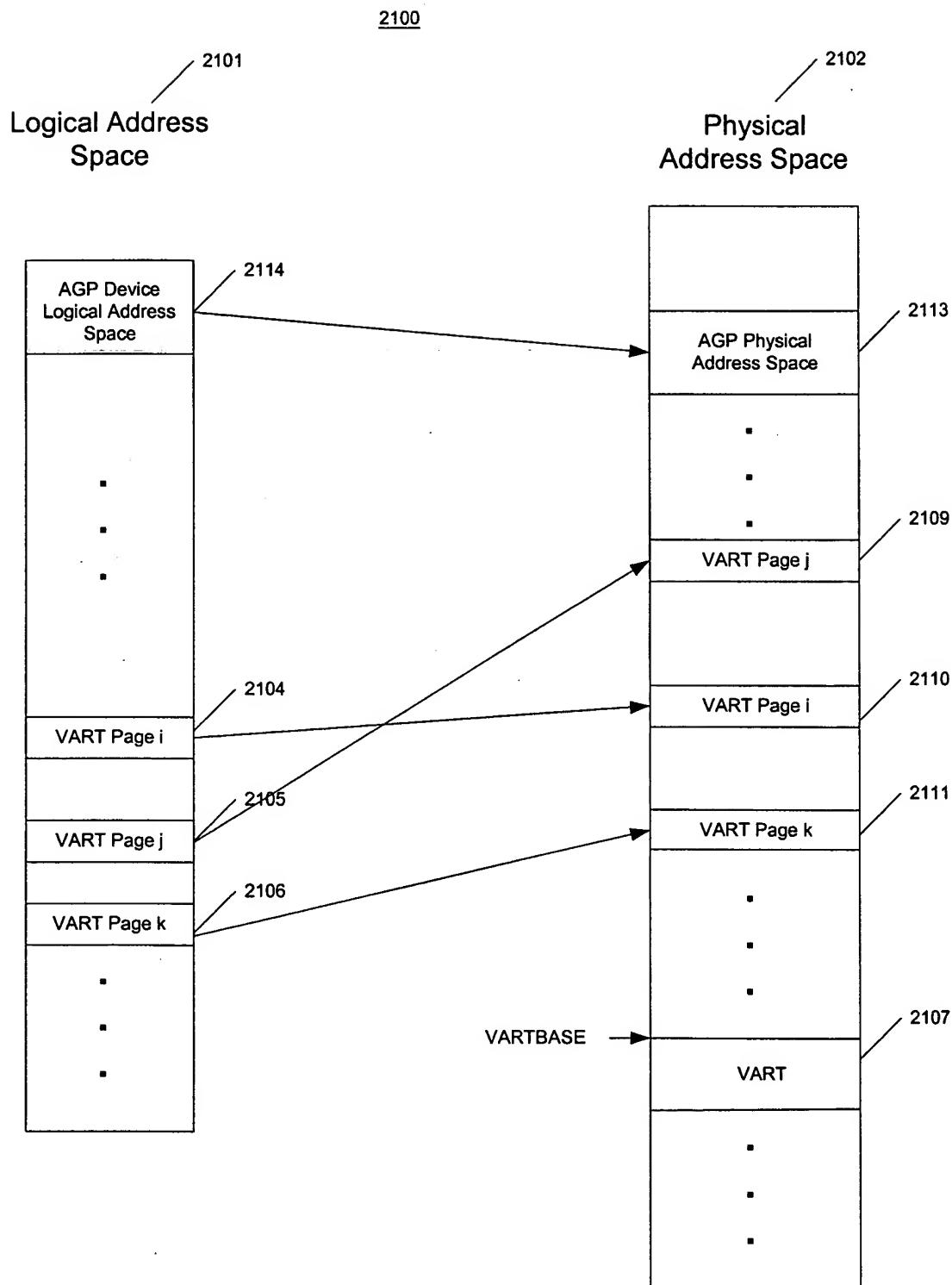
**Figure 9**



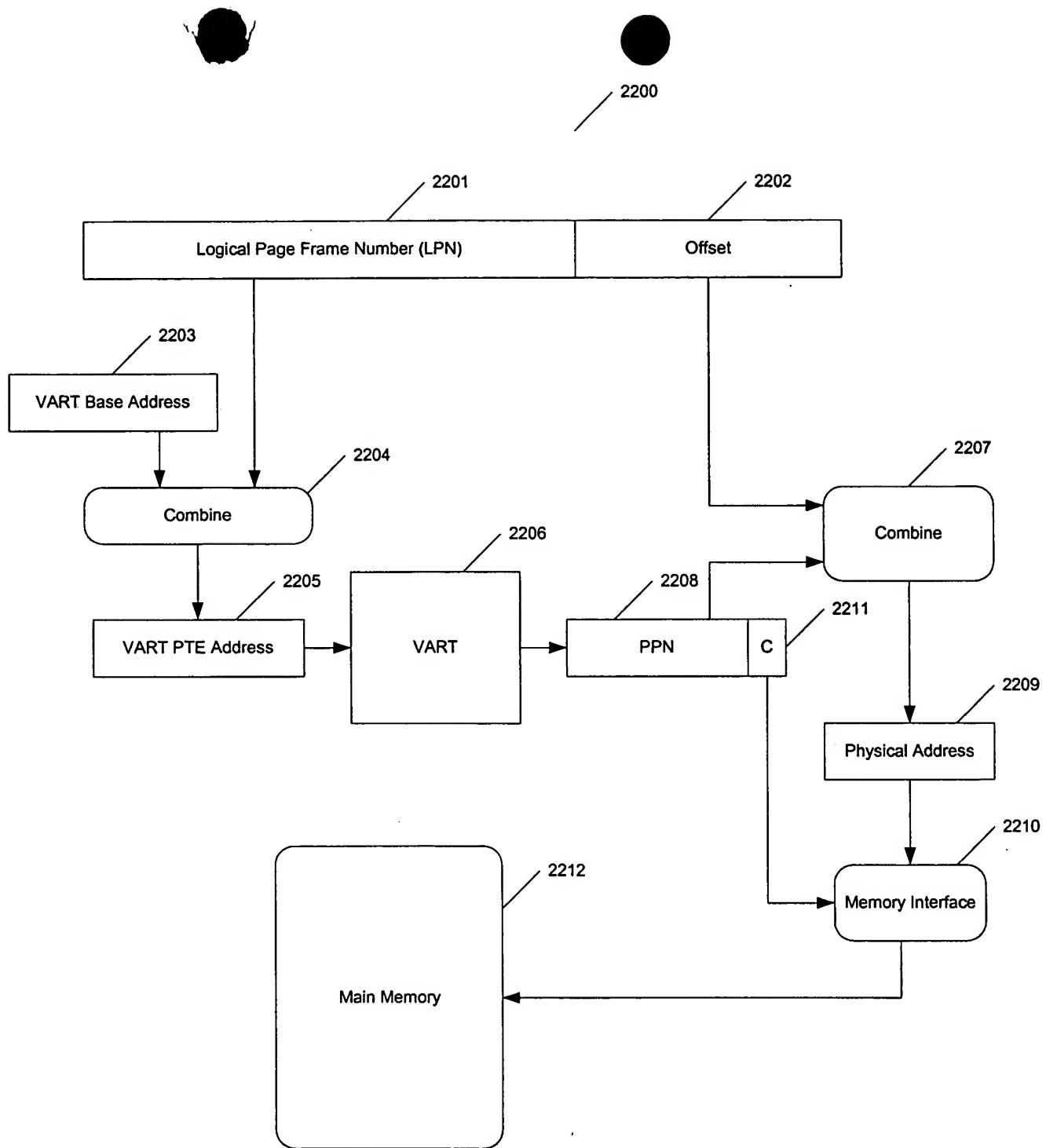
**Figure 10A**



**Figure 10B**



**Figure 11**



**Figure 12**

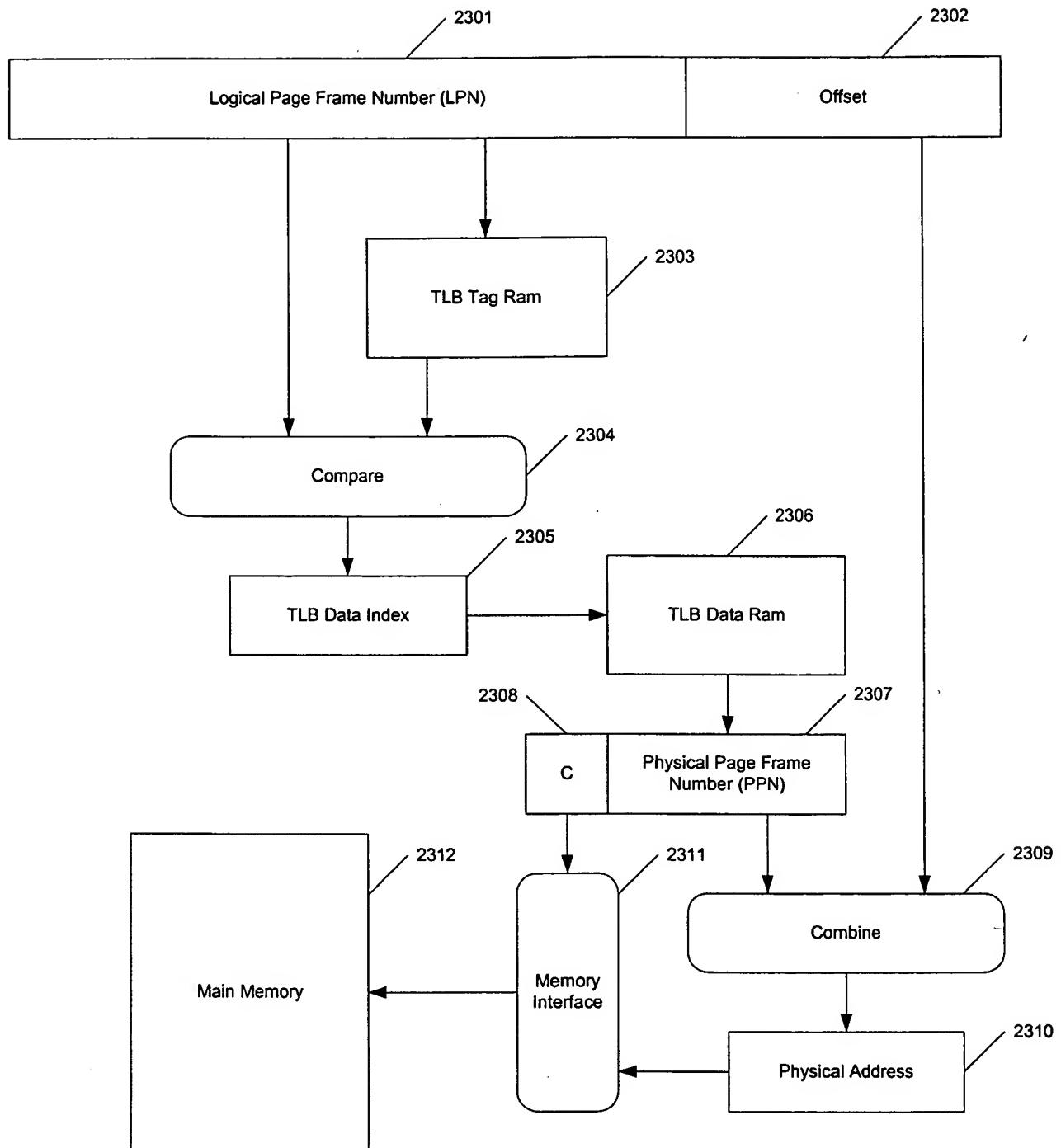


Figure 13

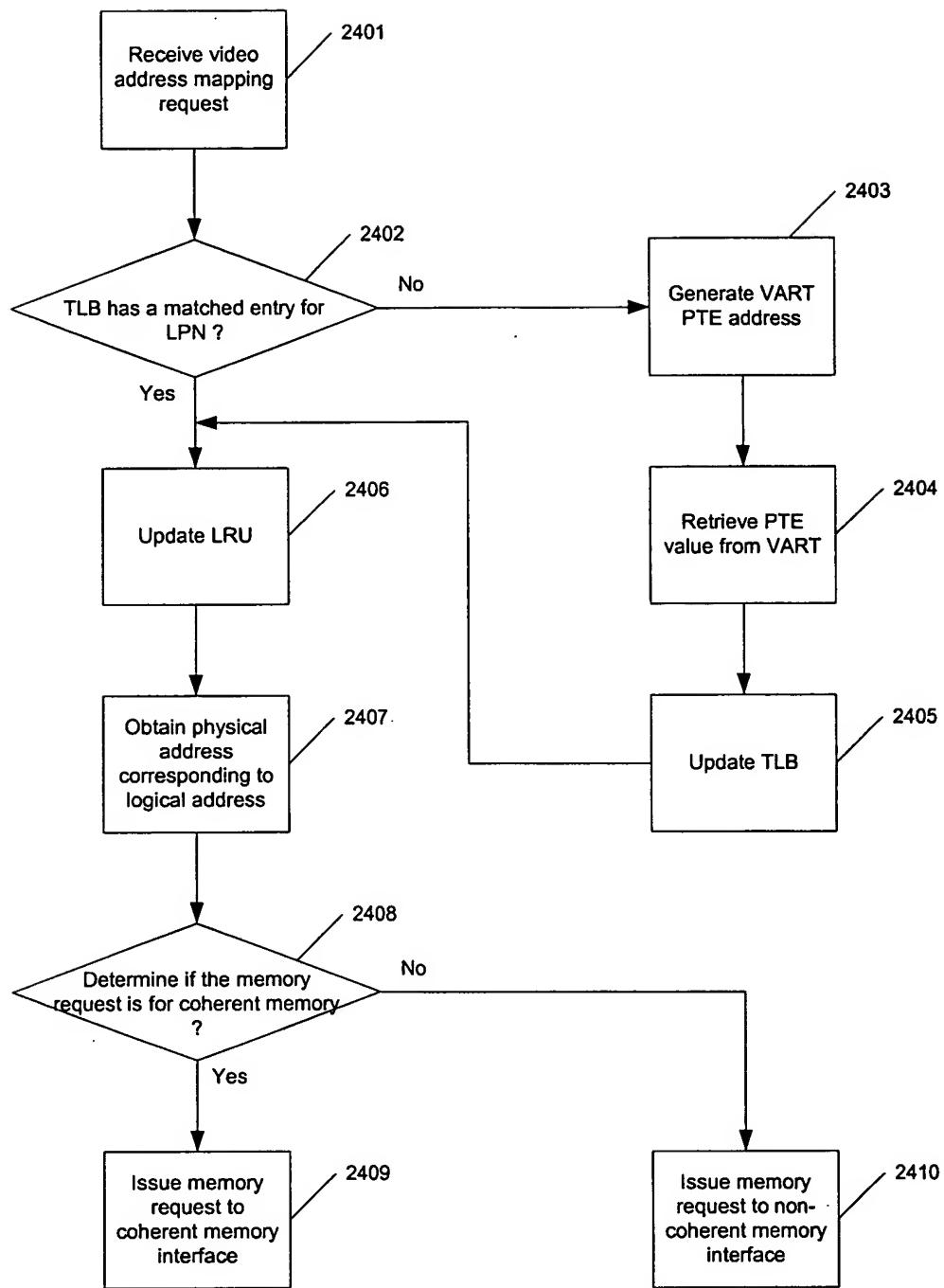


Figure 14

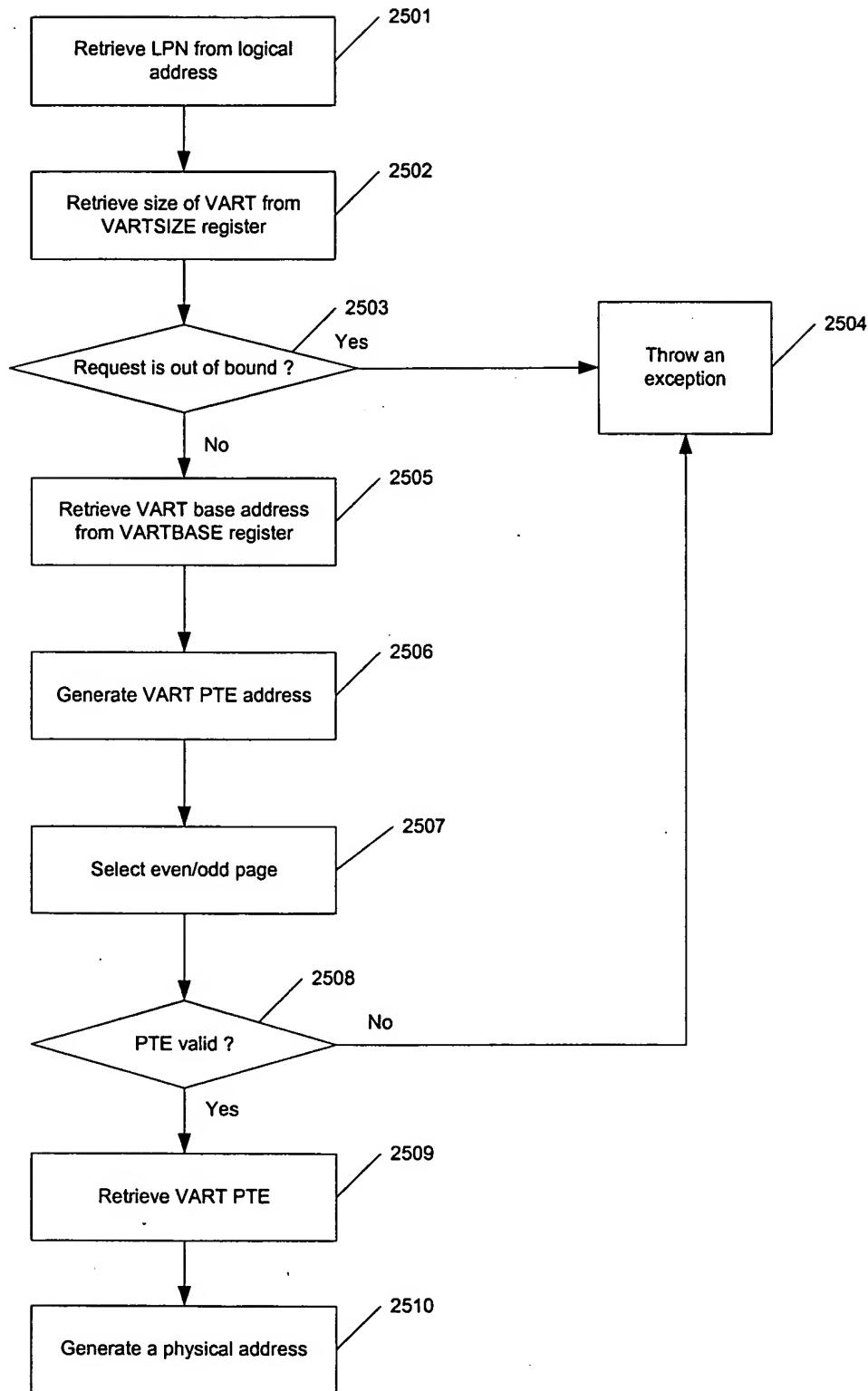


Figure 15

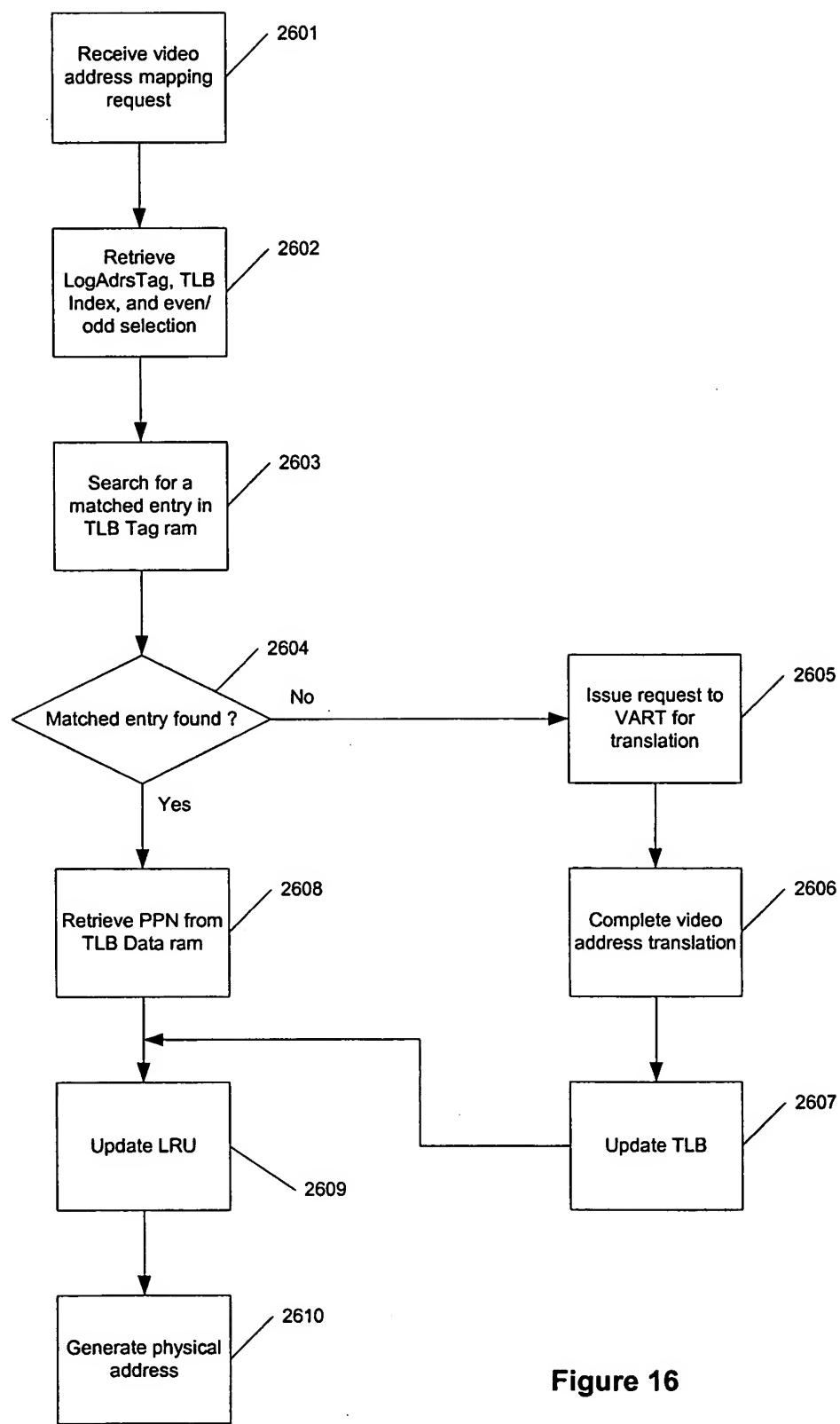
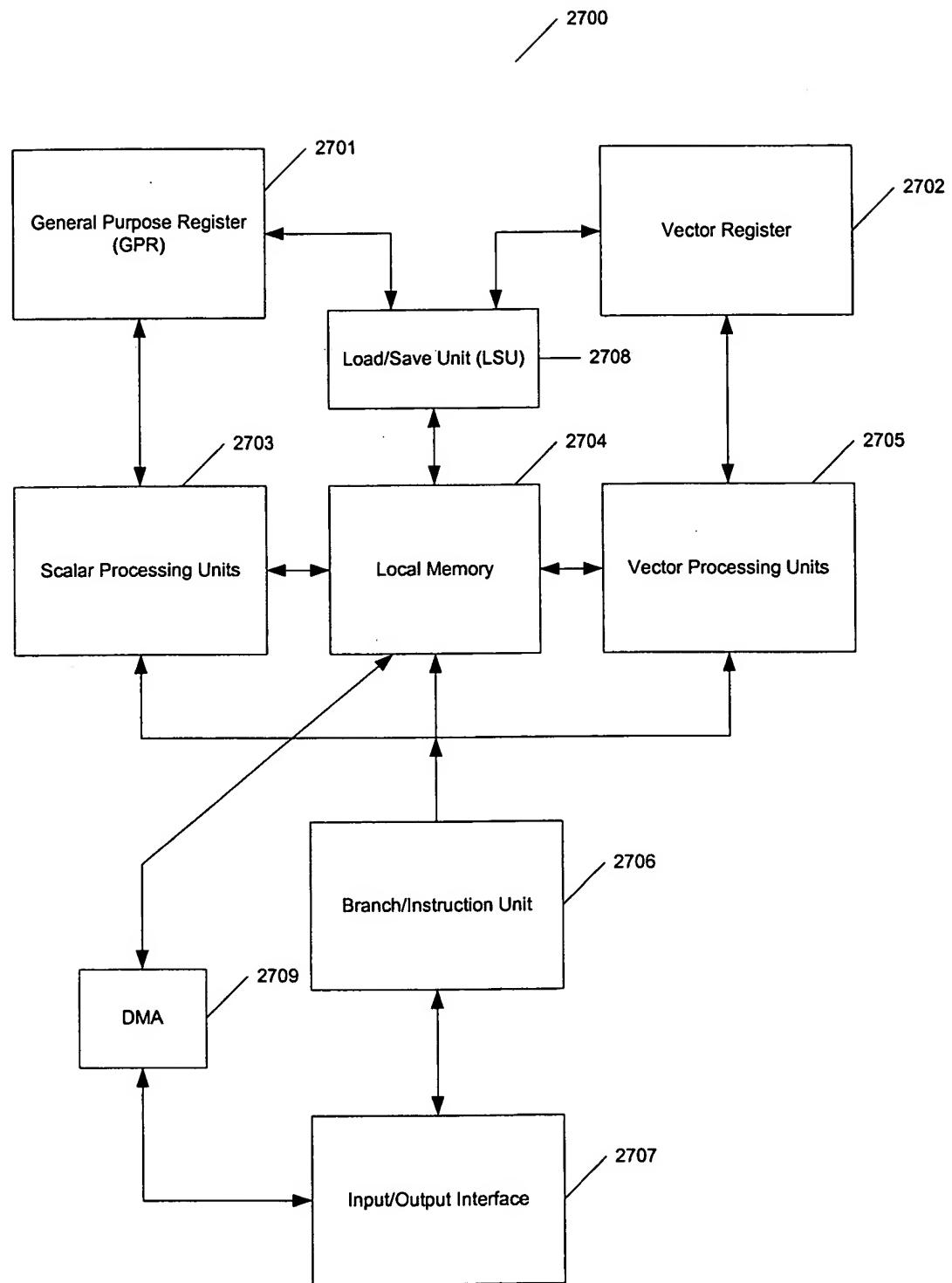
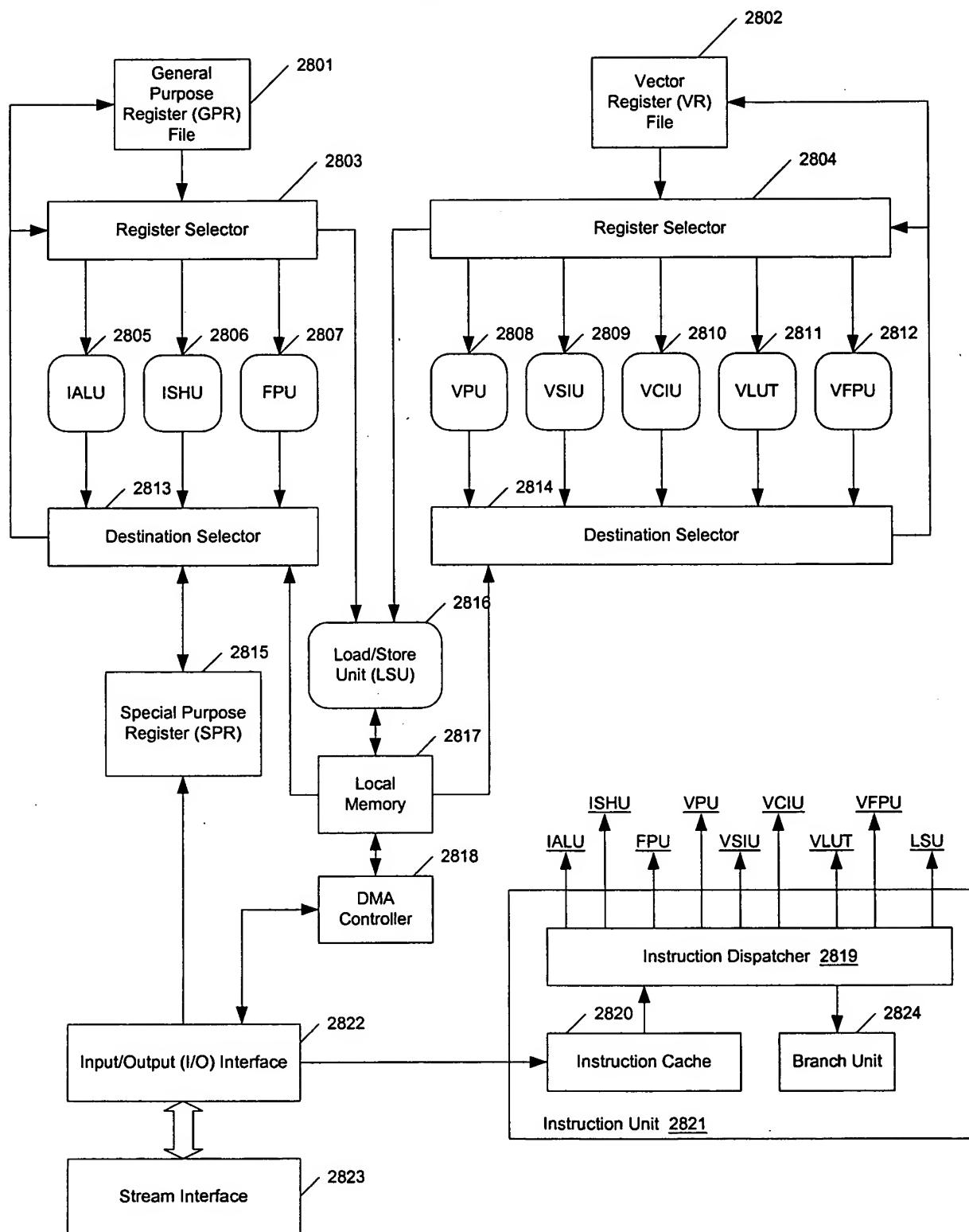


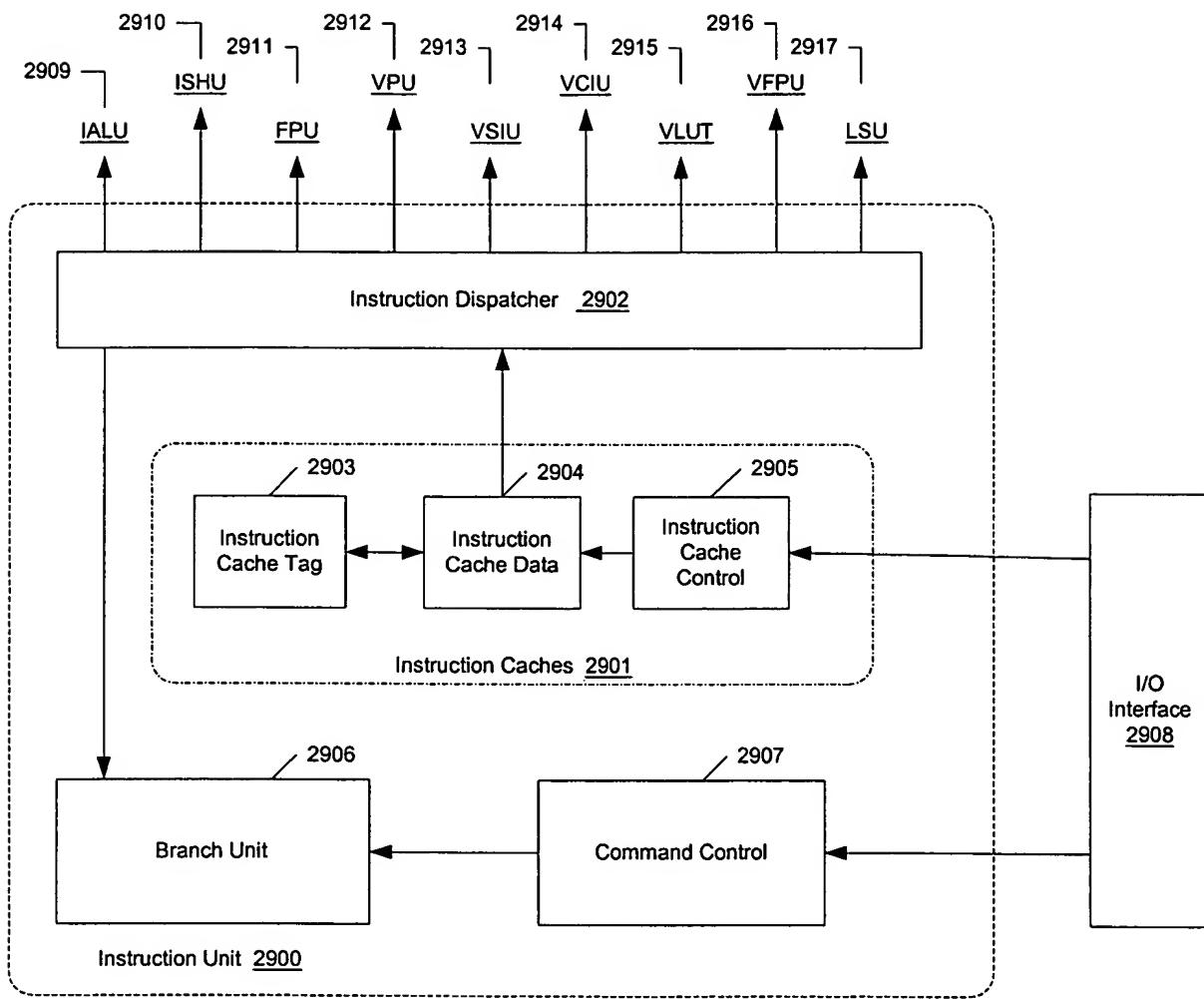
Figure 16



**Figure 17**



**Figure 18**



**Figure 19A**

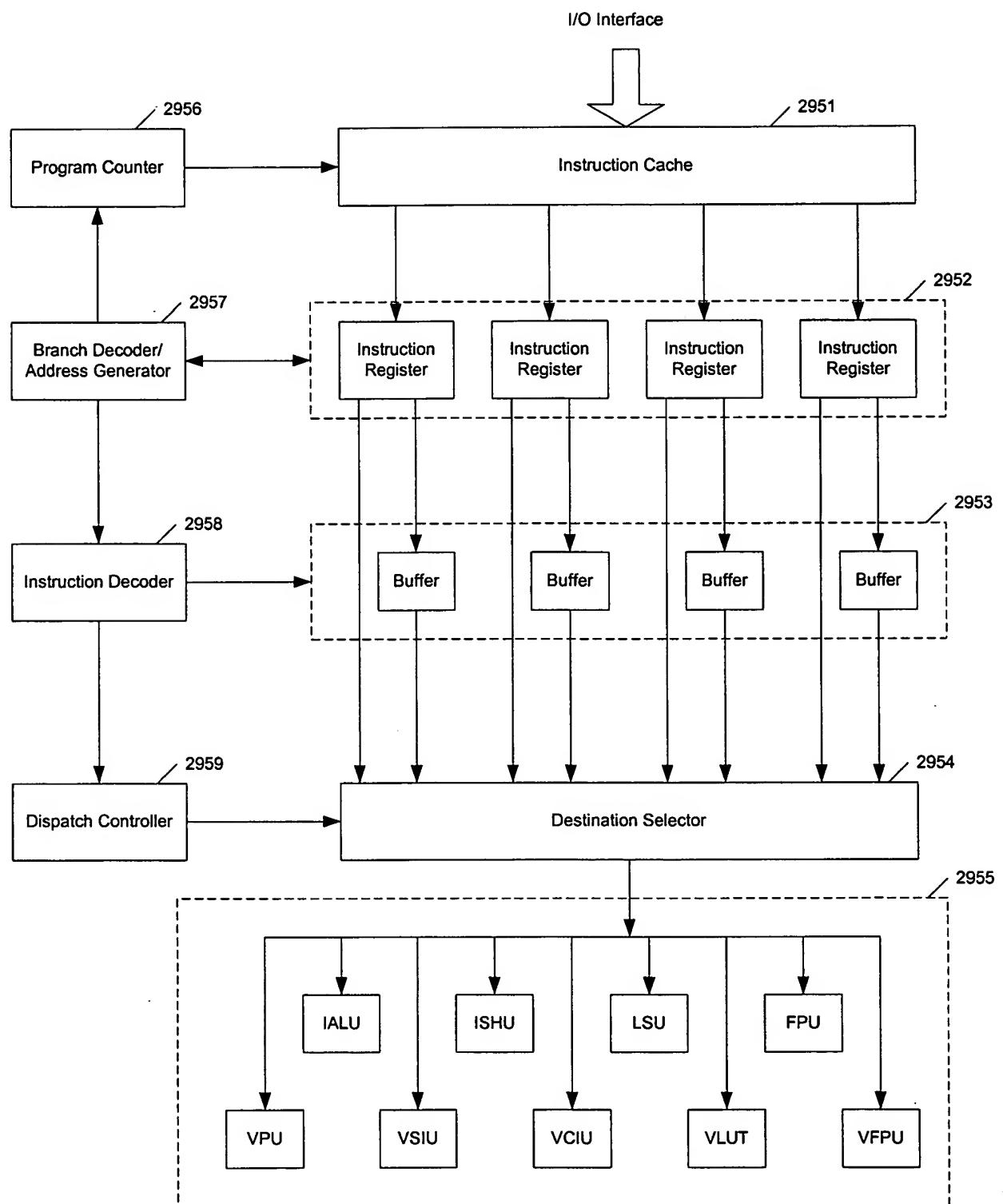
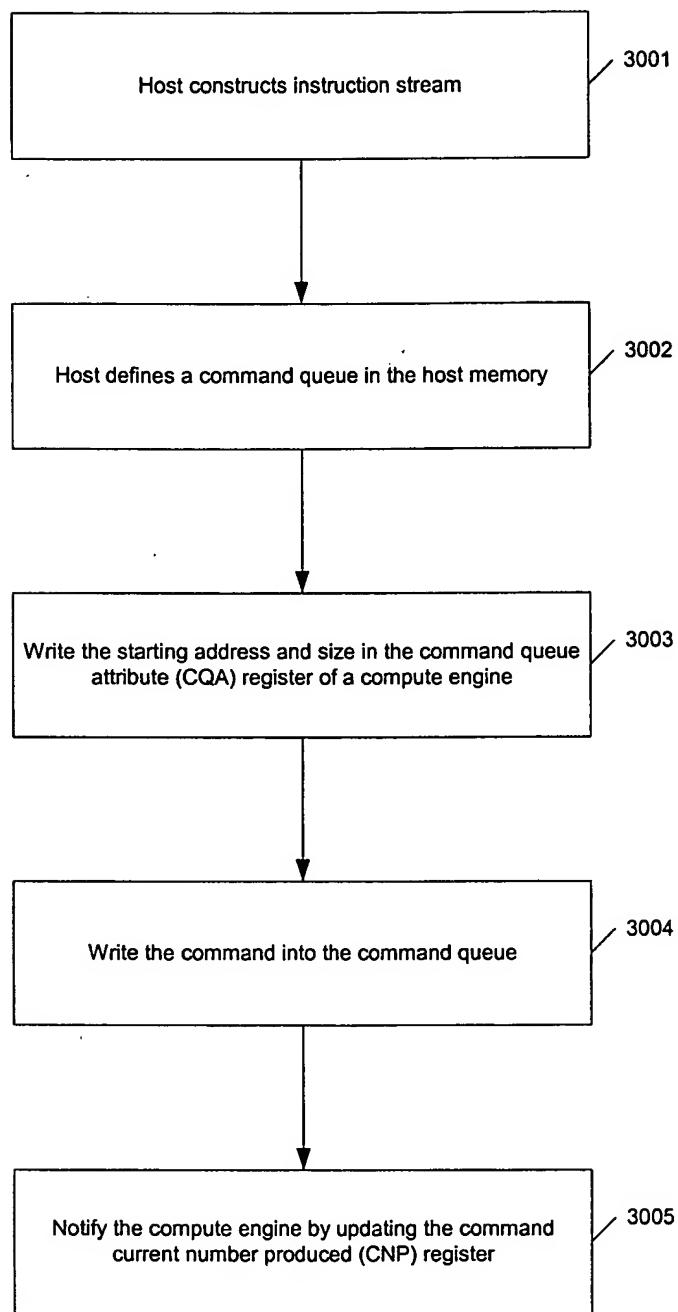


Figure 19B



**Figure 20A**

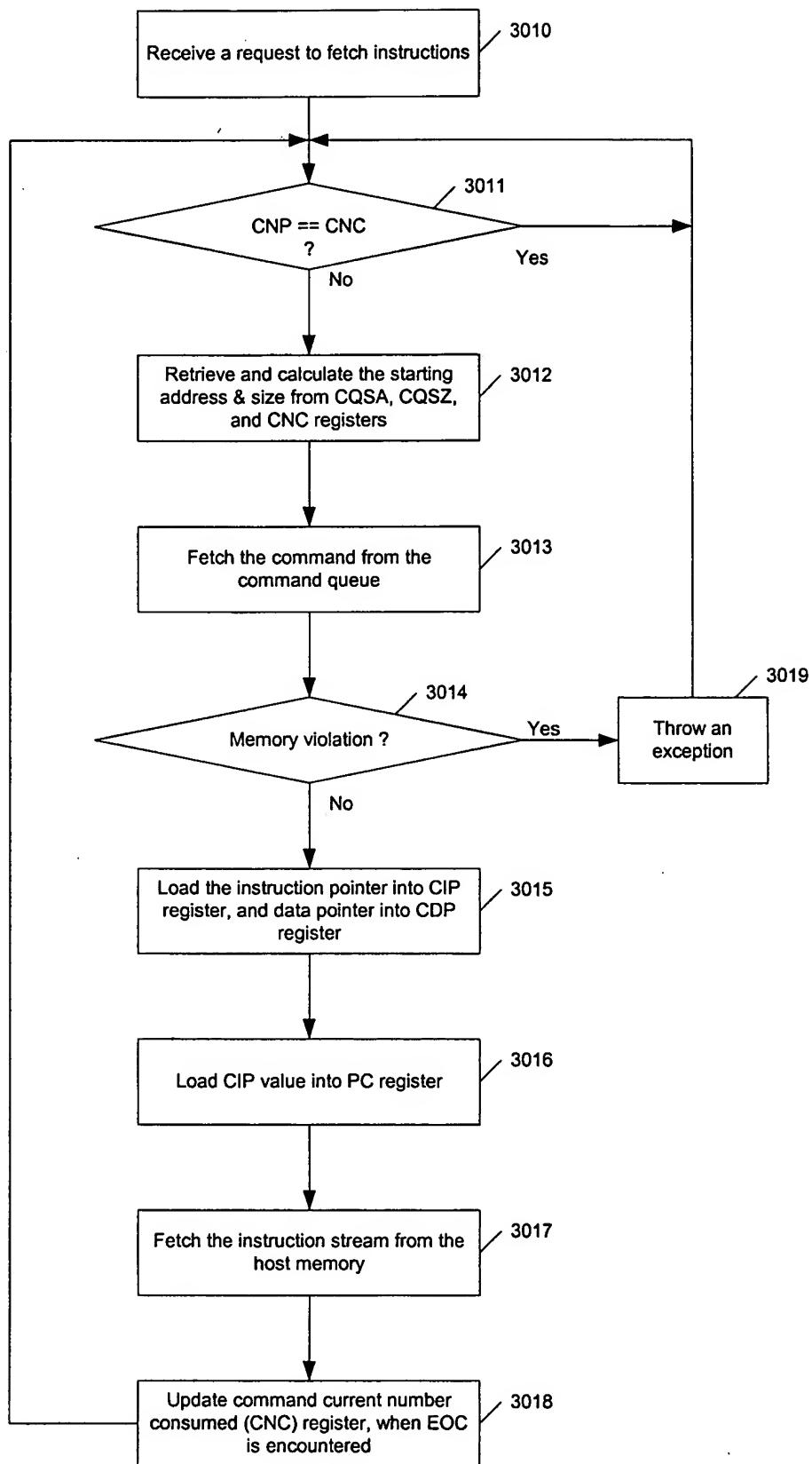


Figure 20B

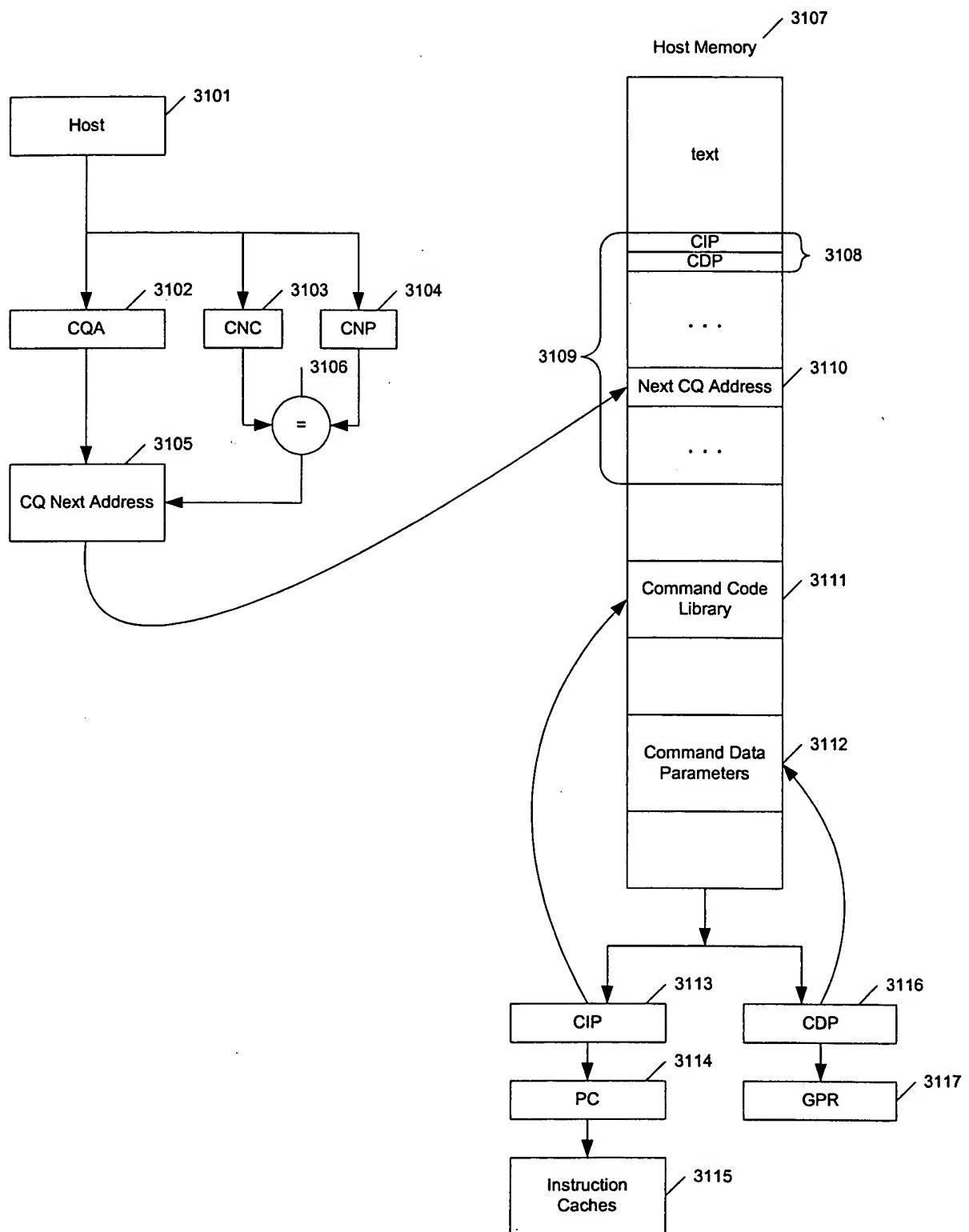


Figure 21

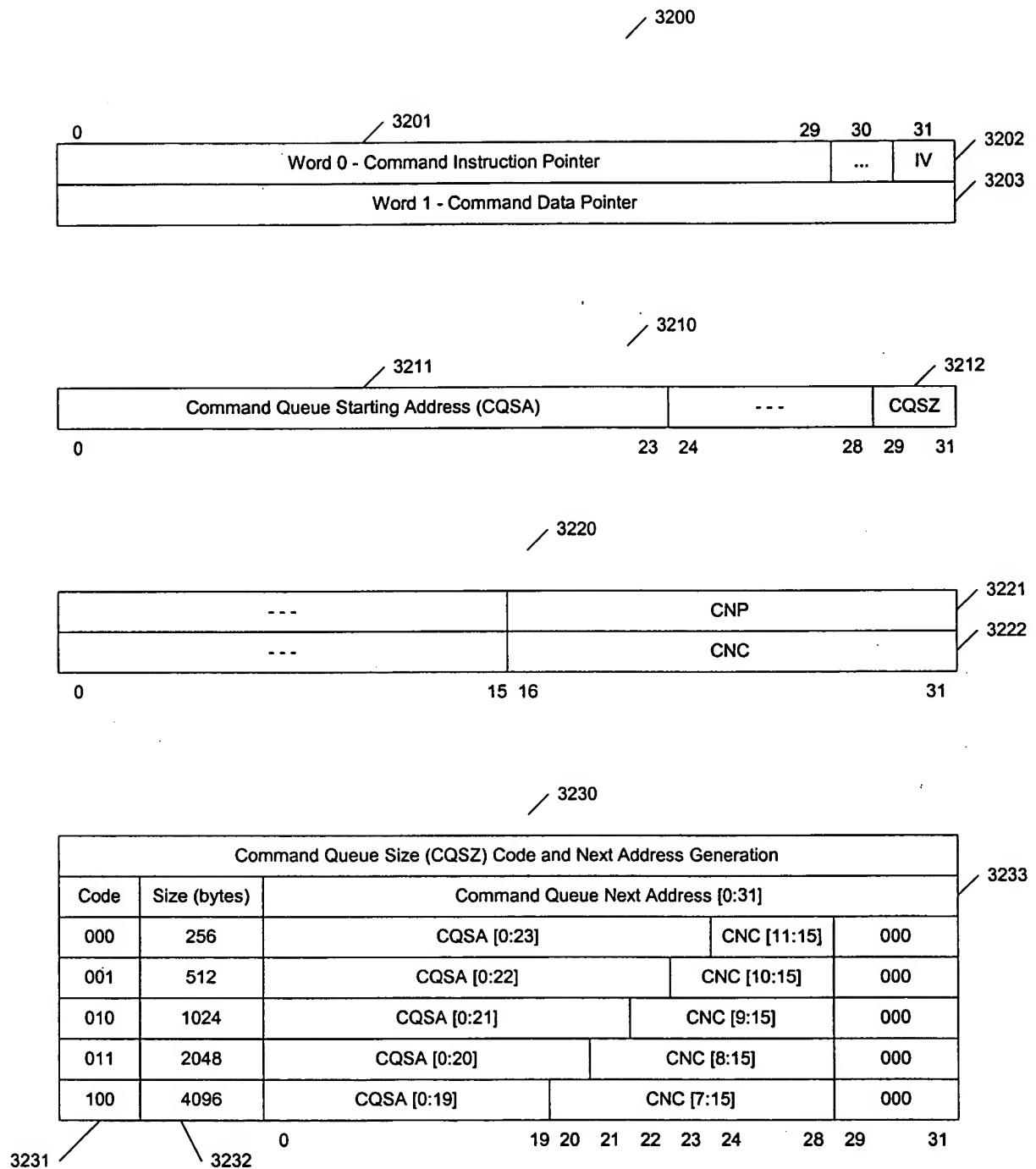


Figure 22

3300

Priority Number	Functional Group Name	3301
0	IALU - Integer Arithmetic/Logical Unit	
1	ISHU - Integer Shift Unit	
2	LSU - Load/Store Unit	
3	VPU - Vector Permute Unit	
4	VSIU - Vector Simple Integer Unit	
5	VCIU - Vector Complex Integer Unit	
6	VLUT - Vector Look-up Table Unit	
7	BRU - Branch Unit	3302

**Figure 23**

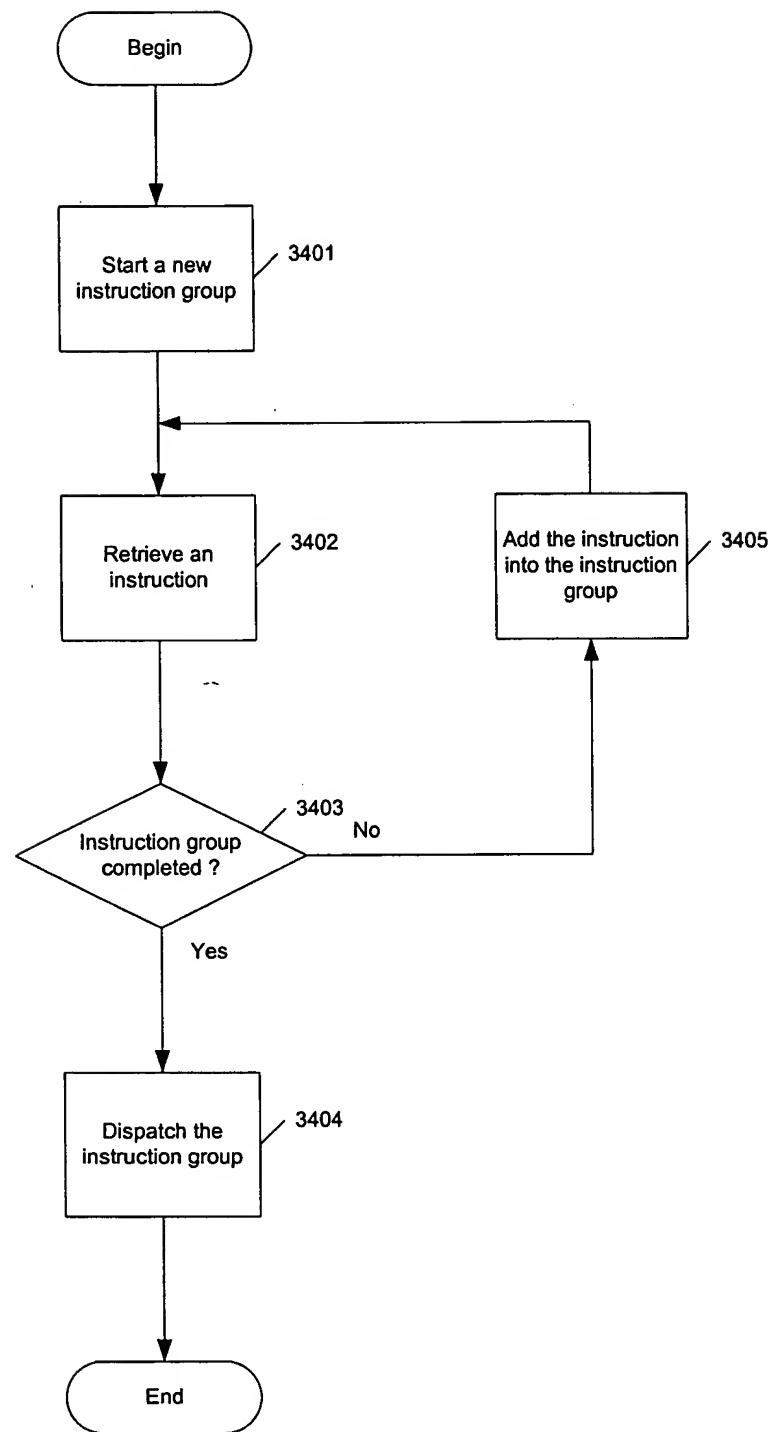


Figure 24

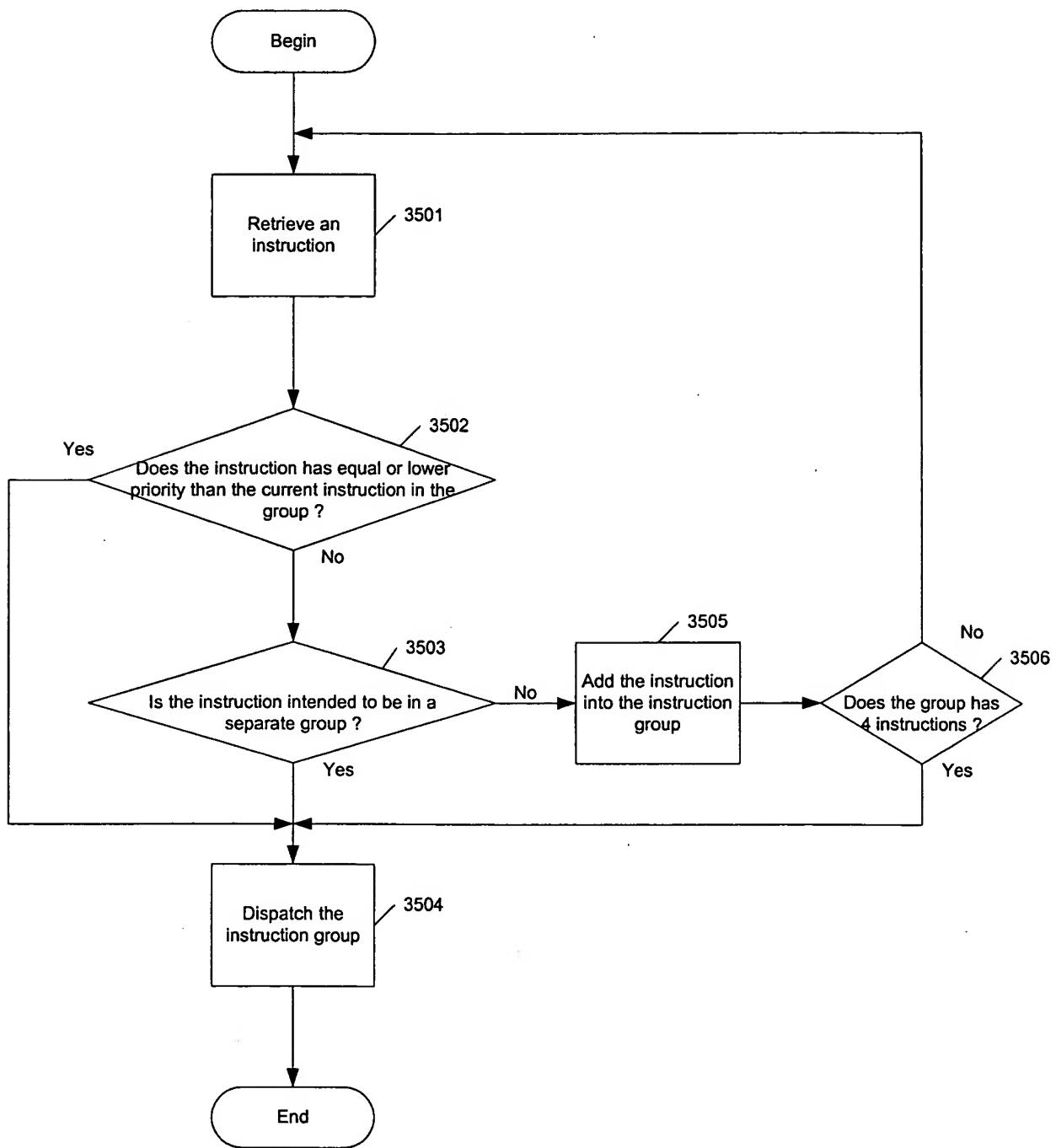
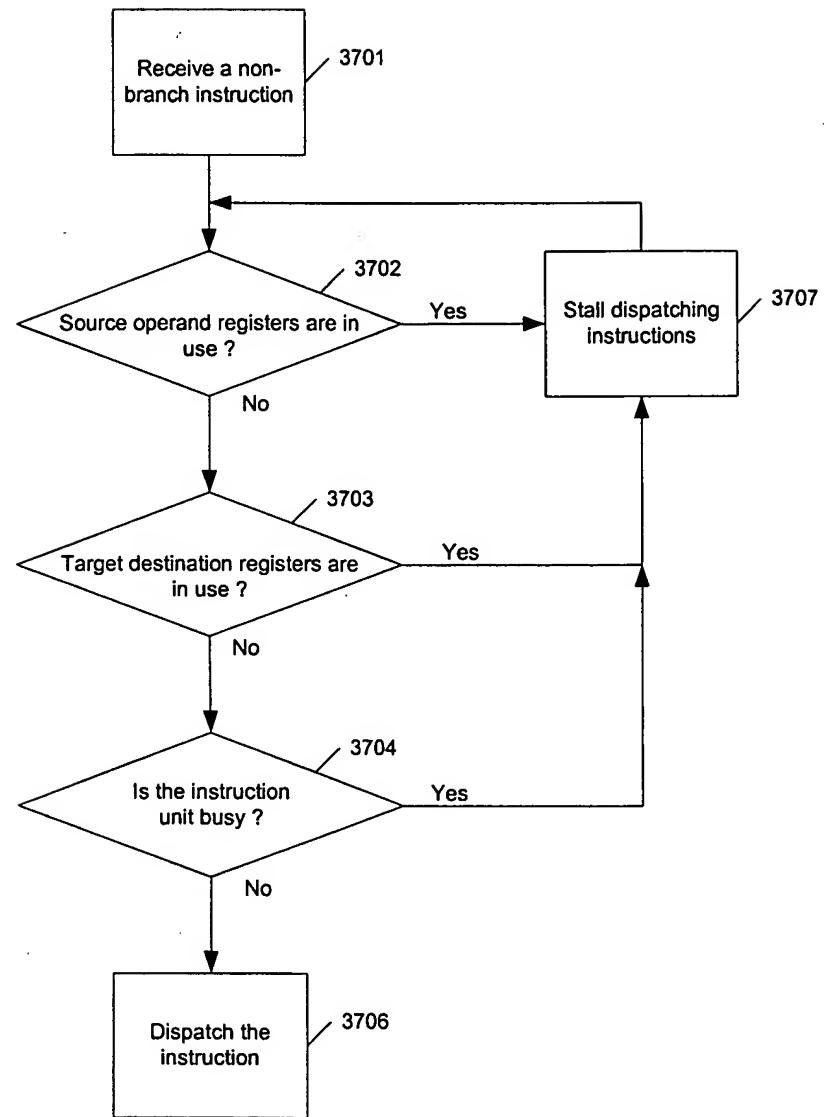


Figure 25

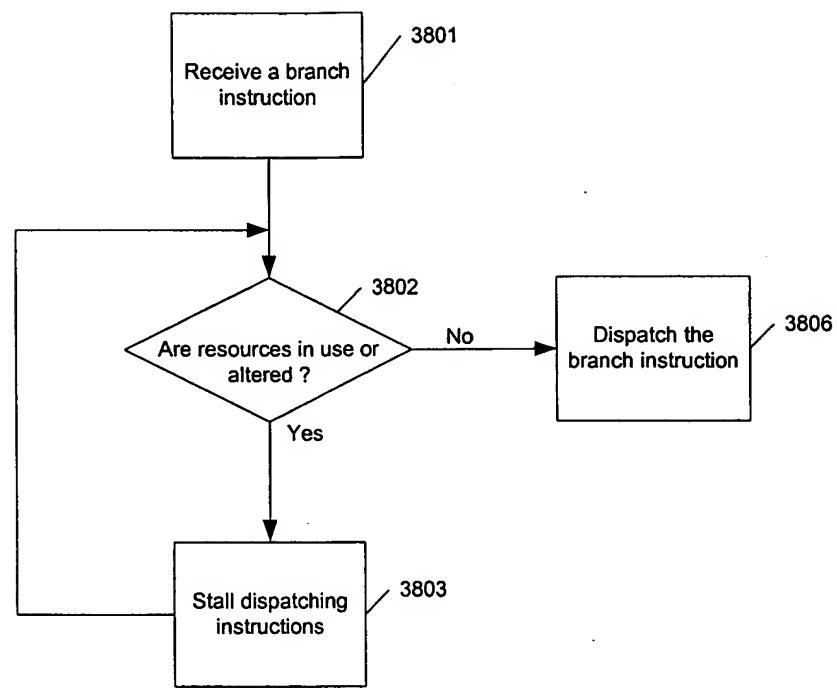
3600

Functional Unit	Latency	Dispatch Rate
IALU - not multiply or divide	2	1
IALU - multiply	19	19
IALU - divide	35	35
ISHU	2	1
LSU - non-DMA address update	2	1
LSU - non-DMA load data update	3	1
LSU - non-DMA store	1	1
LSU - DMA instructions	1	1
VPU	2	1
VSIU	2	1
VCIU	6	1
VLUT - reads, vvid	4	1
VLUT - writes	1	1
Branch instruction	1	1

Figure 26



**Figure 27**



**Figure 28**

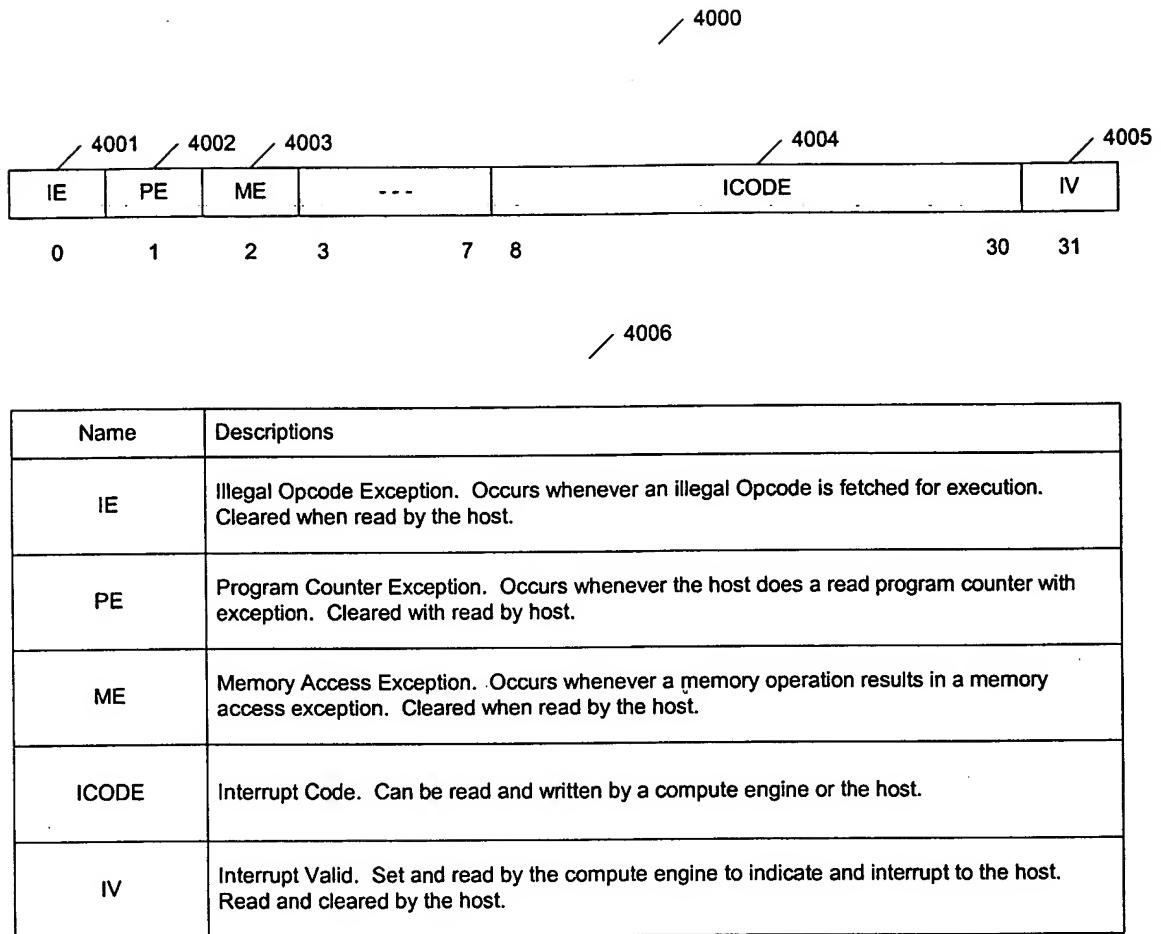
3900

Program Counter	PSt
0	29 30 31

3901

Pst	Name	Description
00	Idle	CQ counters are equal and no current command executing. Program counter is invalid.
01	Run	Command was executing. Program counter points to next instruction that would have been executed.
10	IWait	Command was executing, but instruction fetching has stopped due to a previous exception. Program counter points to the next instruction that would have been executed.
11	CWait	Command was not executing due to an exception in fetching the command. Program counter is invalid.

**Figure 29**



**Figure 30**

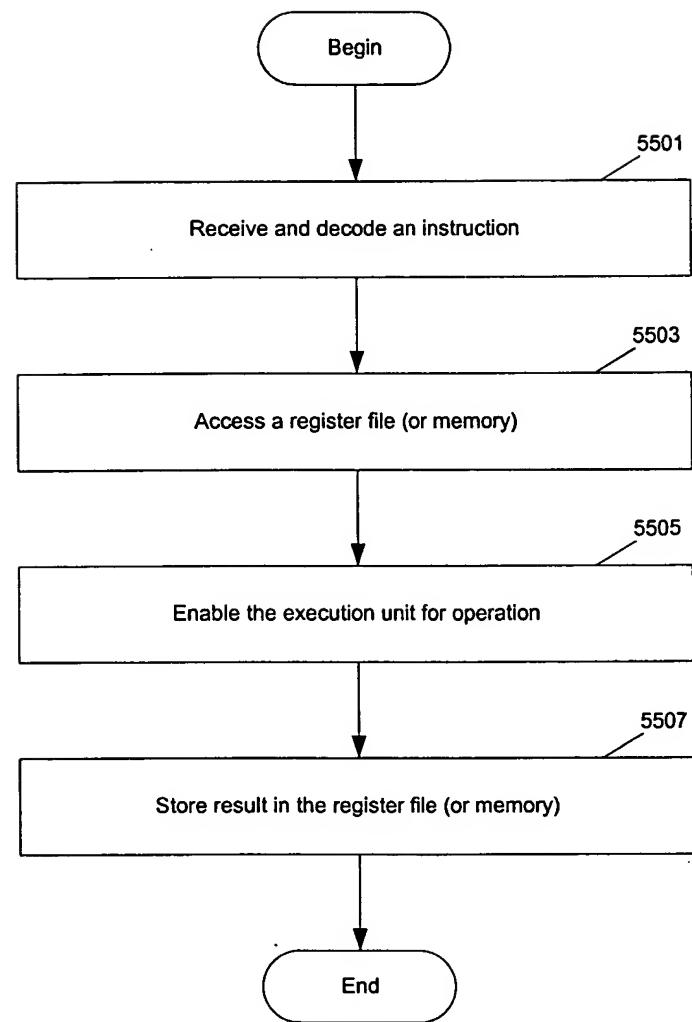


Fig. 31

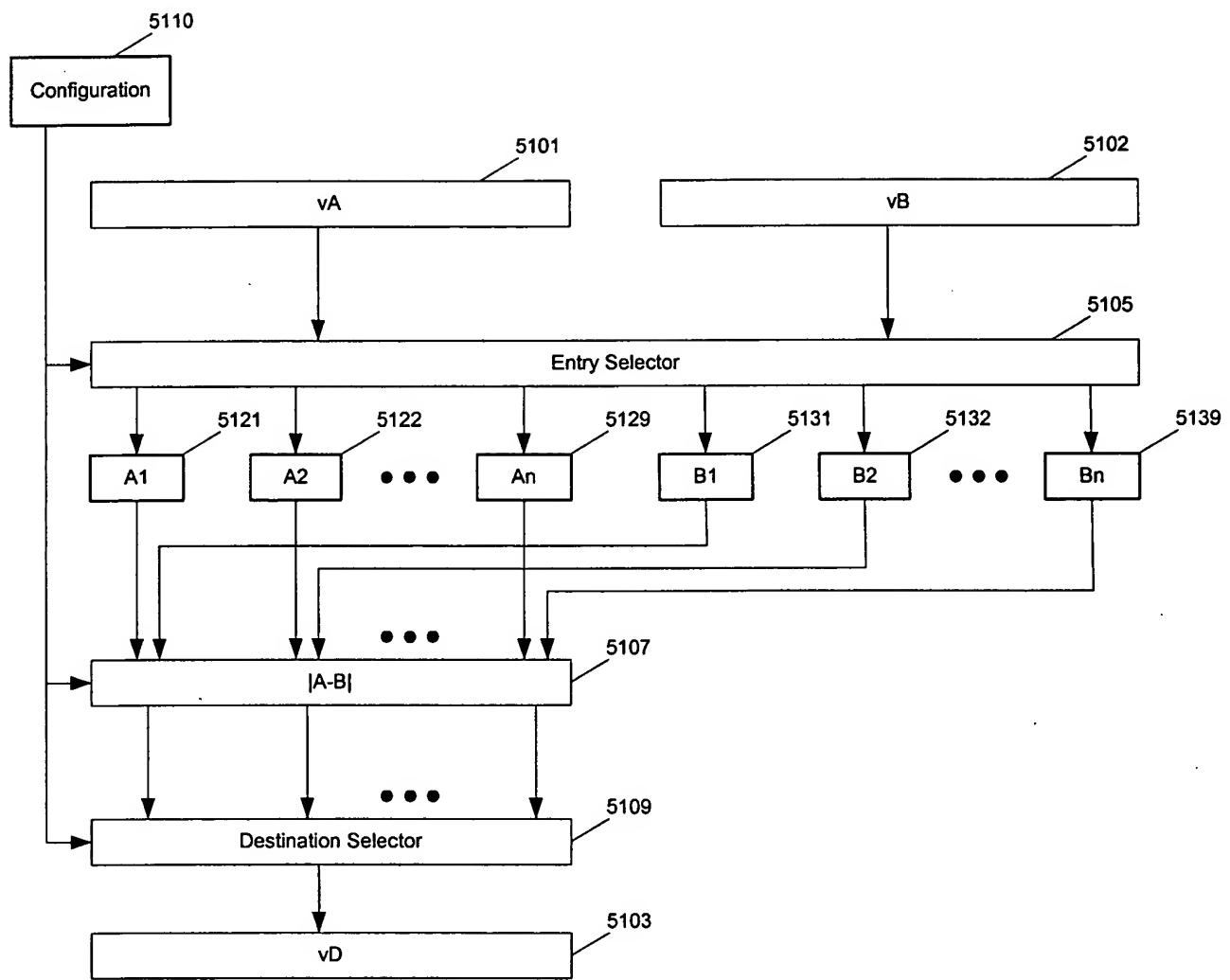


Fig. 32

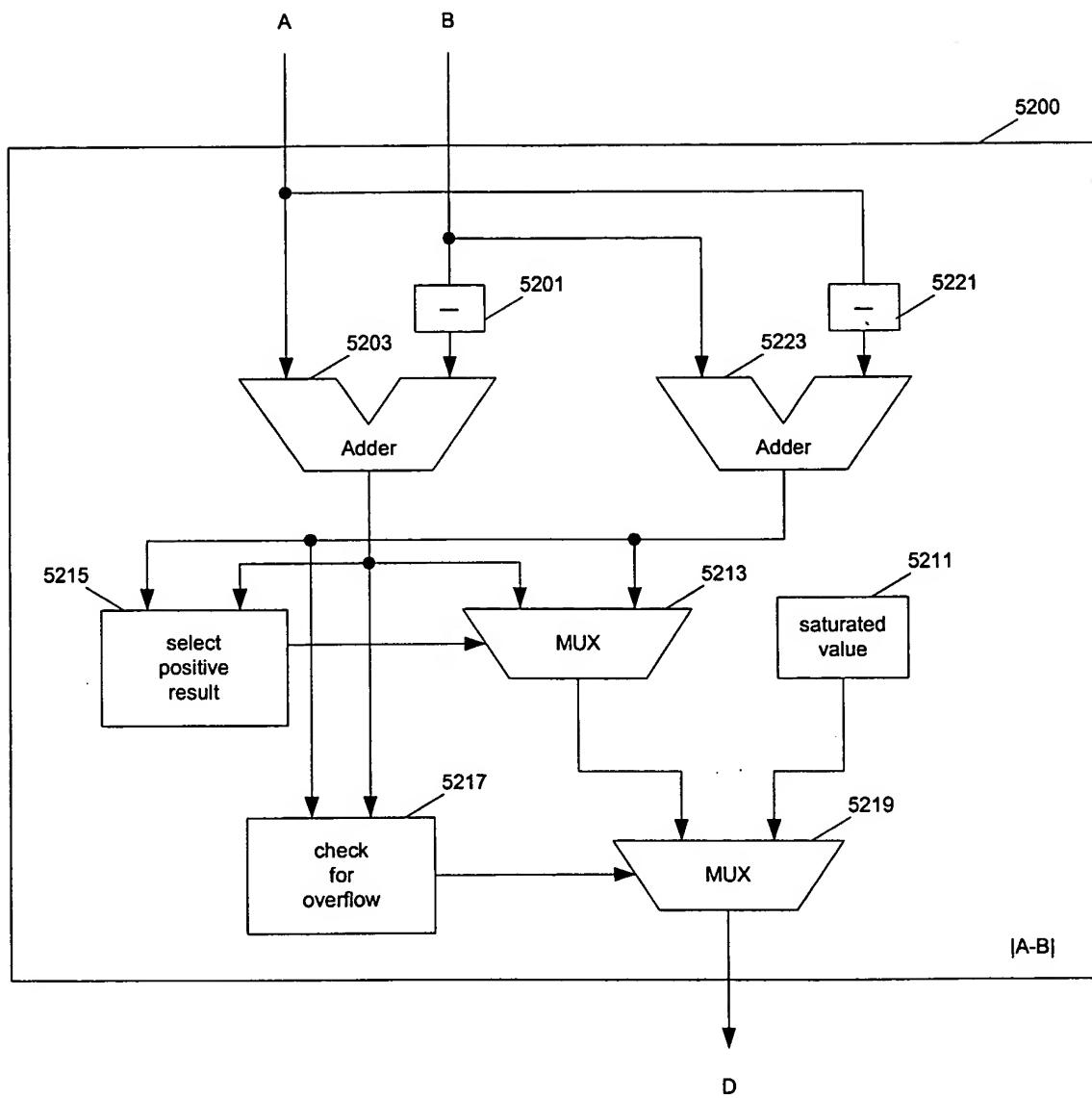


Fig. 33

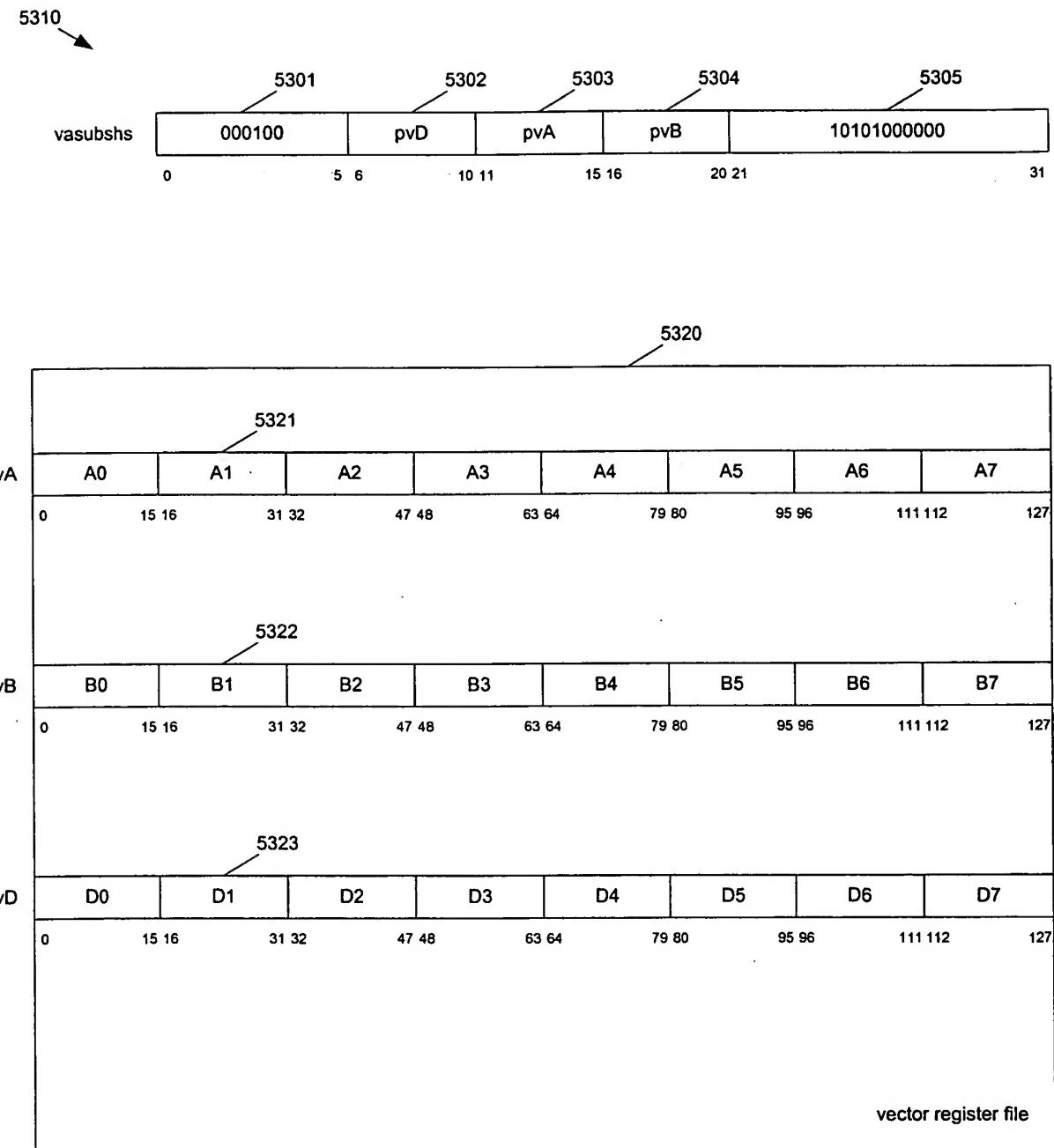


Fig. 34

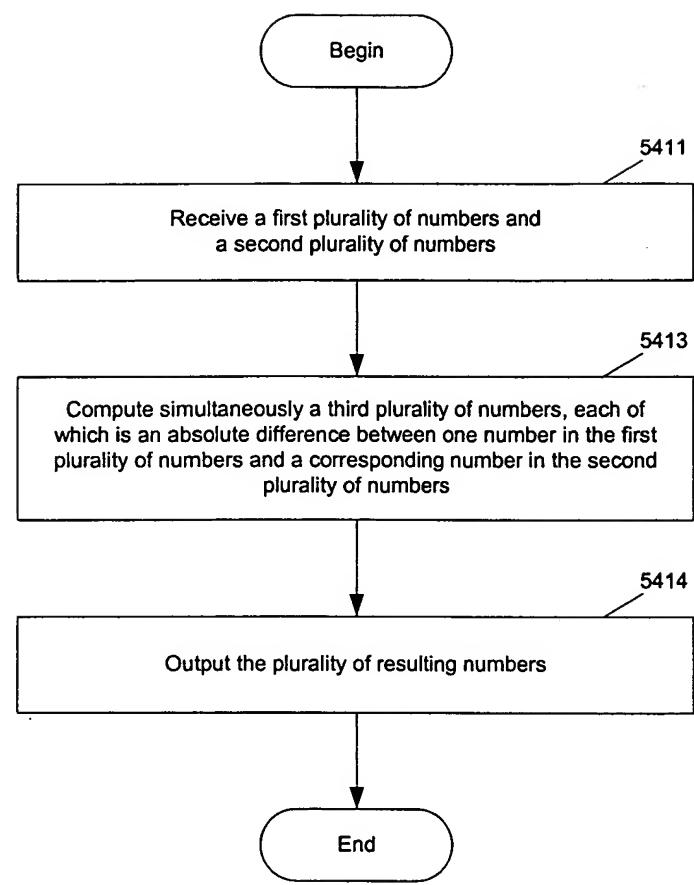


Fig. 35

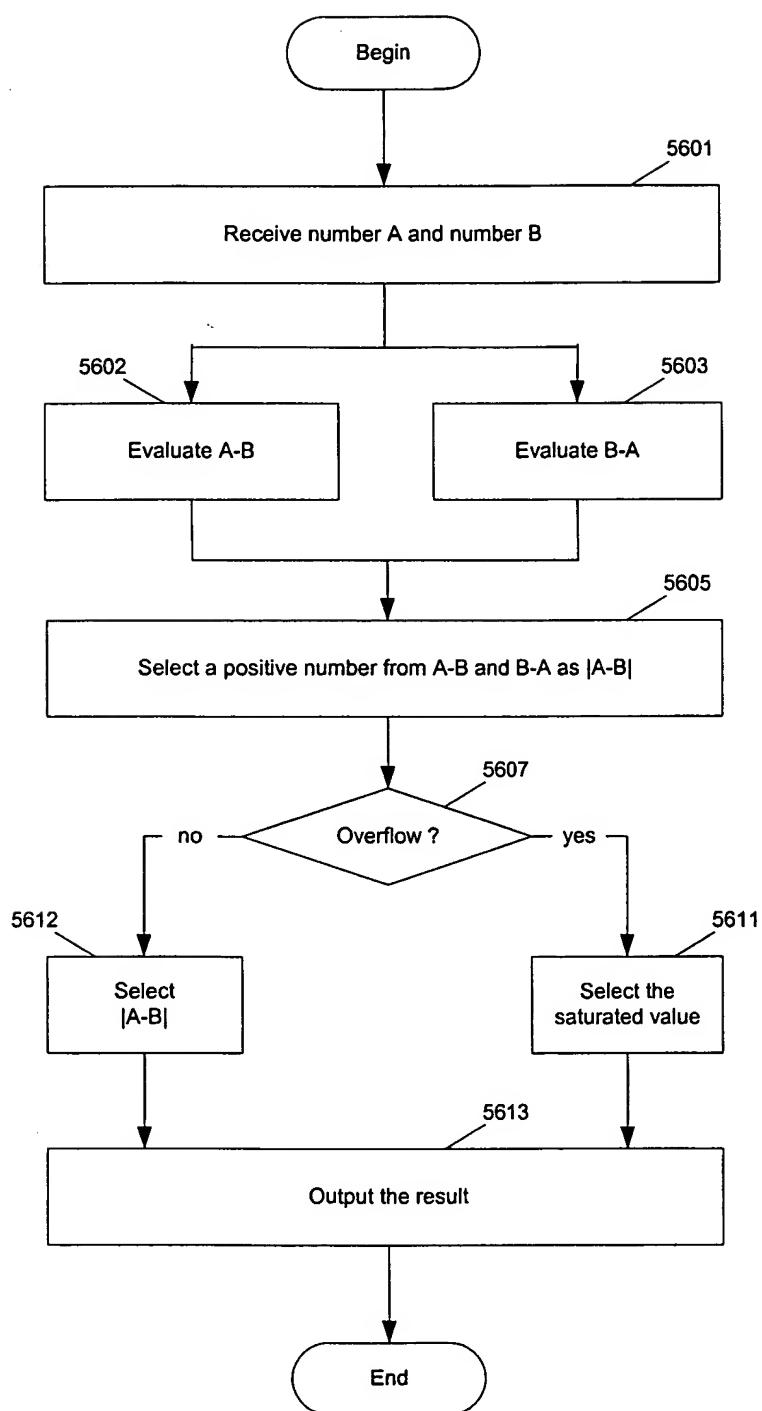


Fig. 36

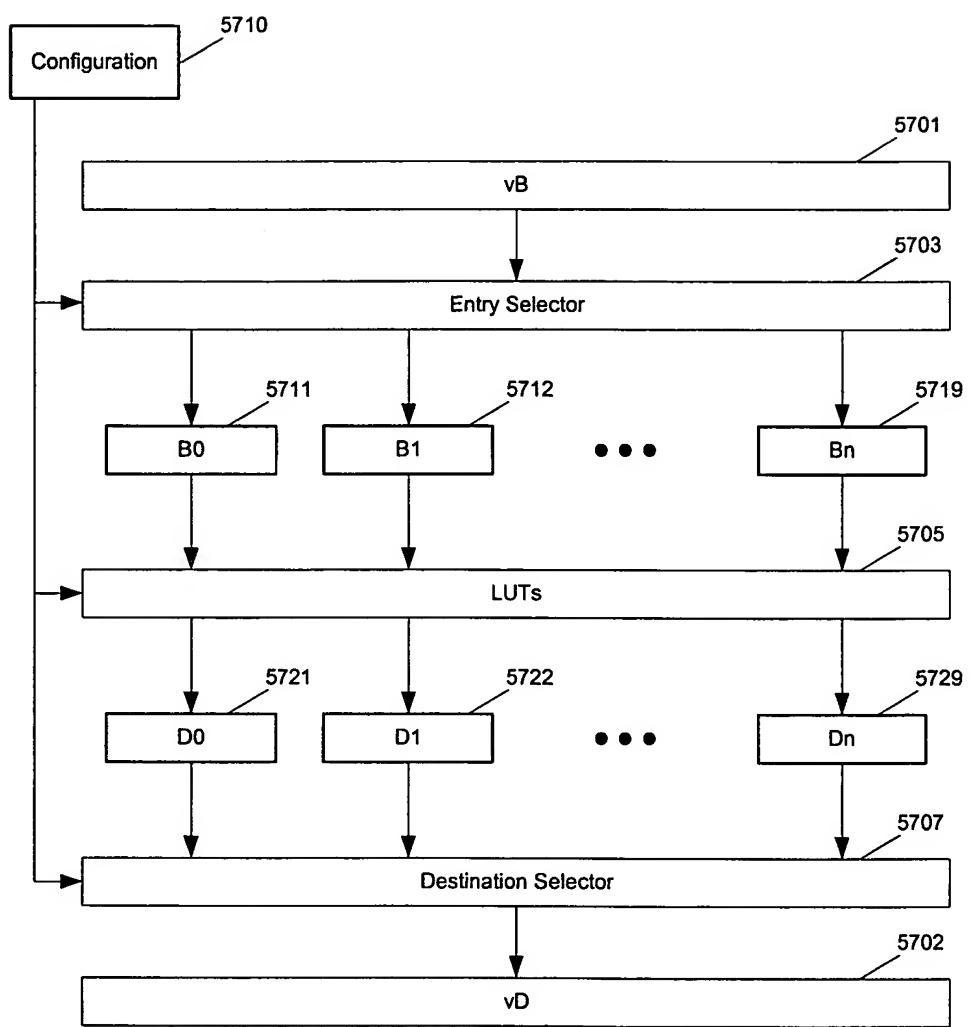


Fig. 37

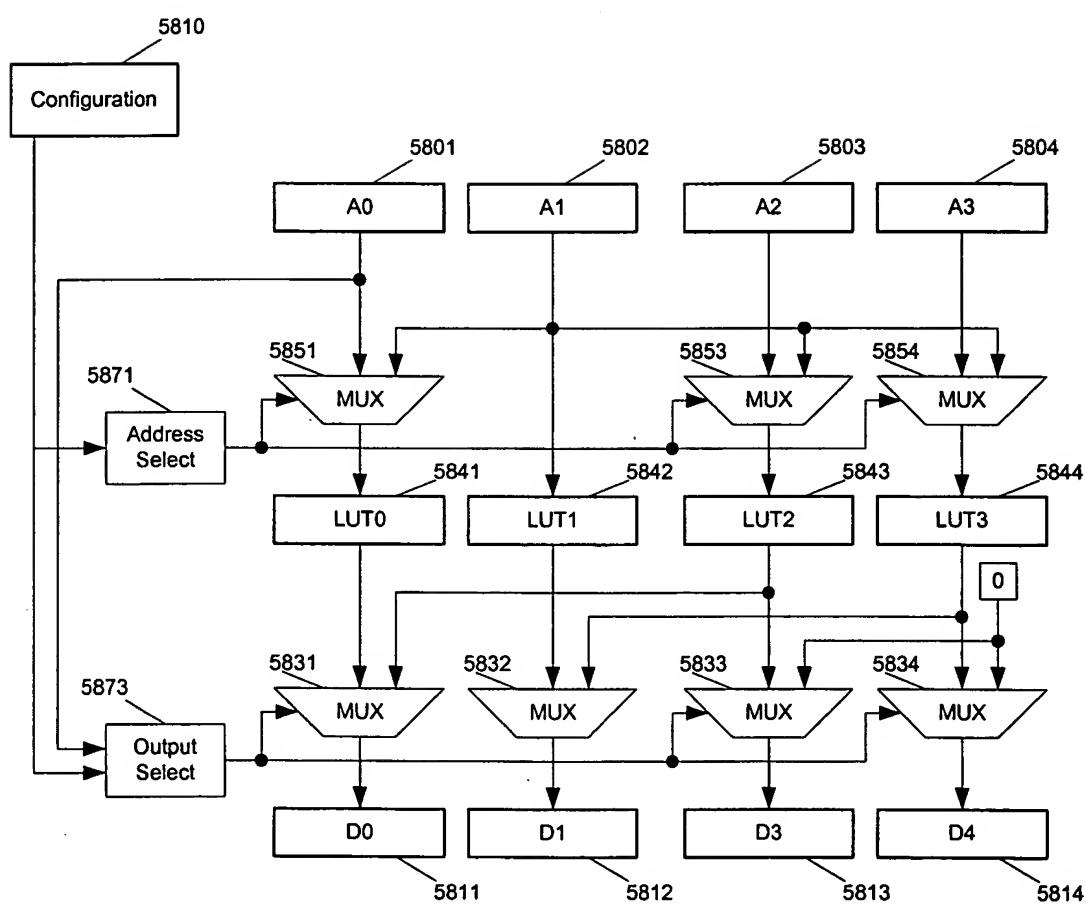


Fig. 38

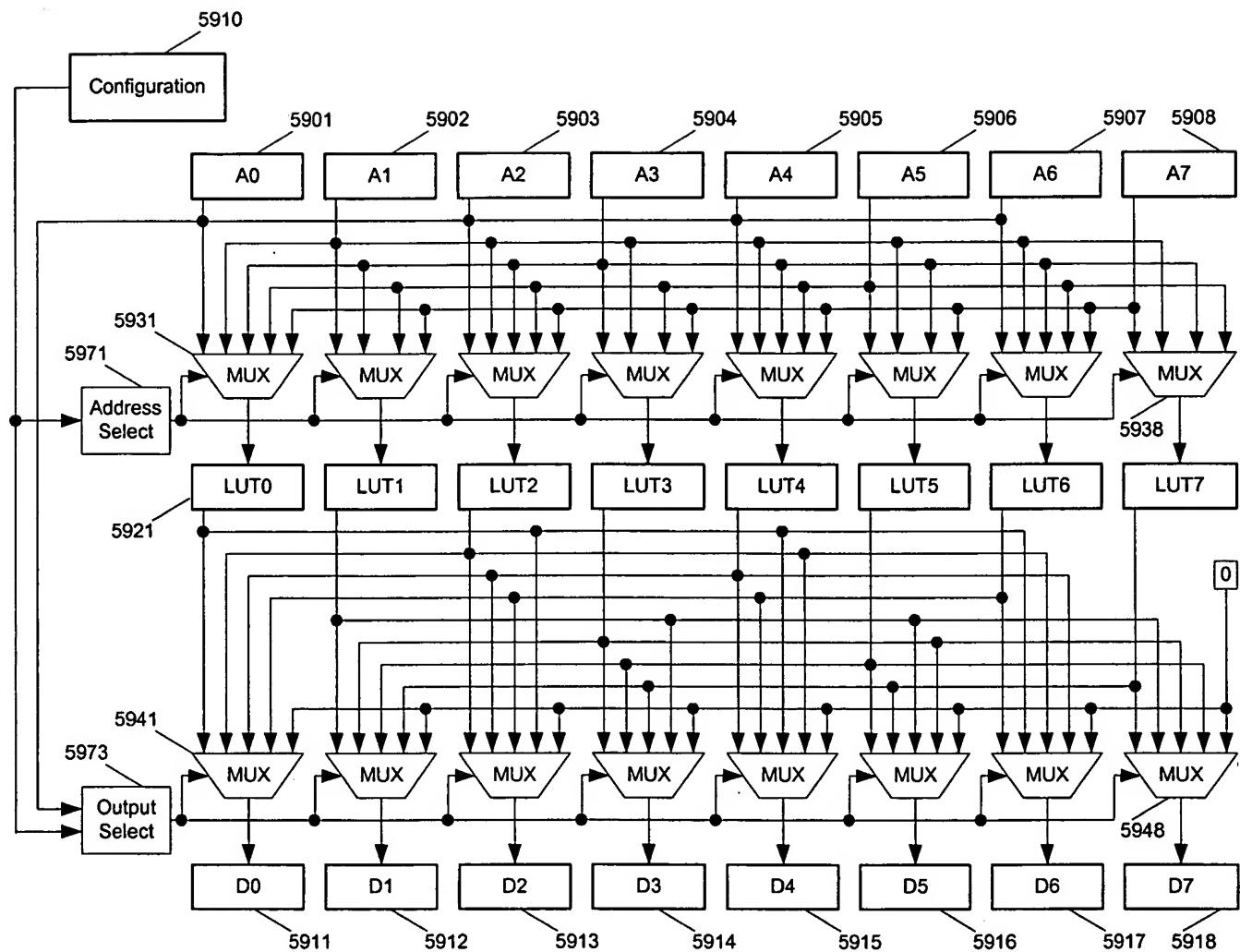


Fig. 39

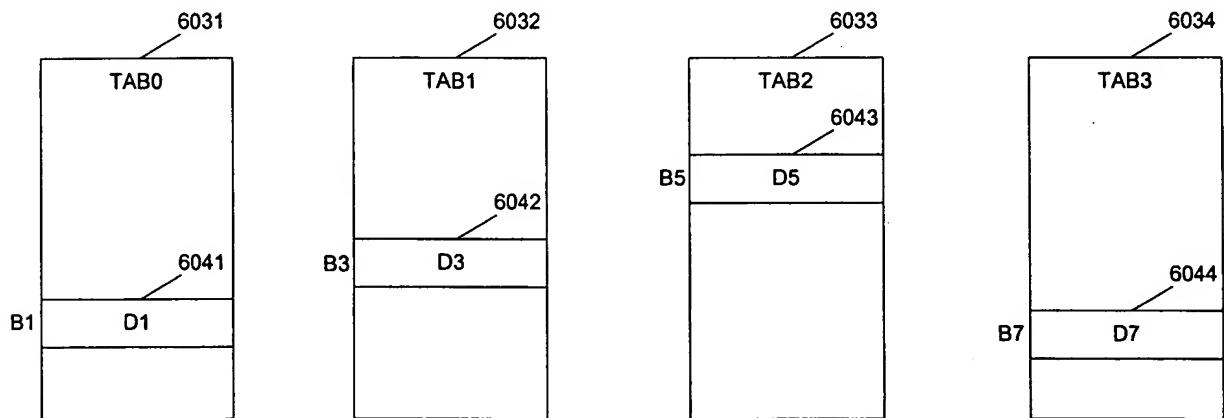
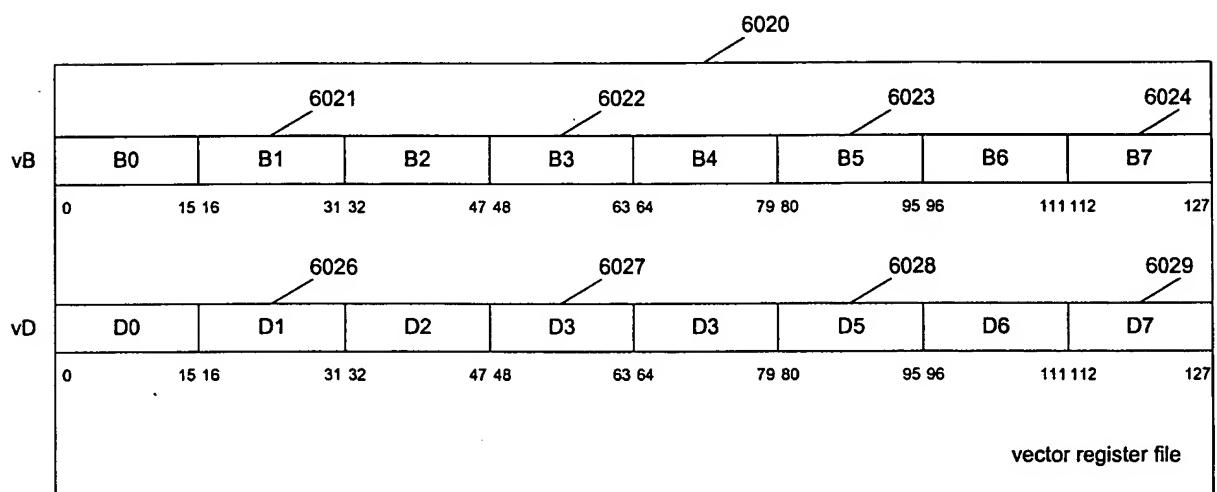
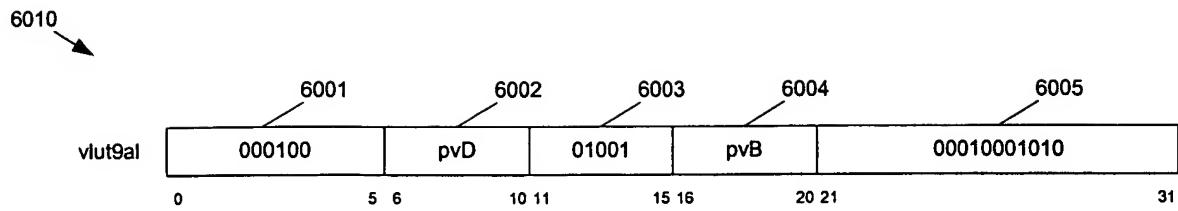


Fig. 40

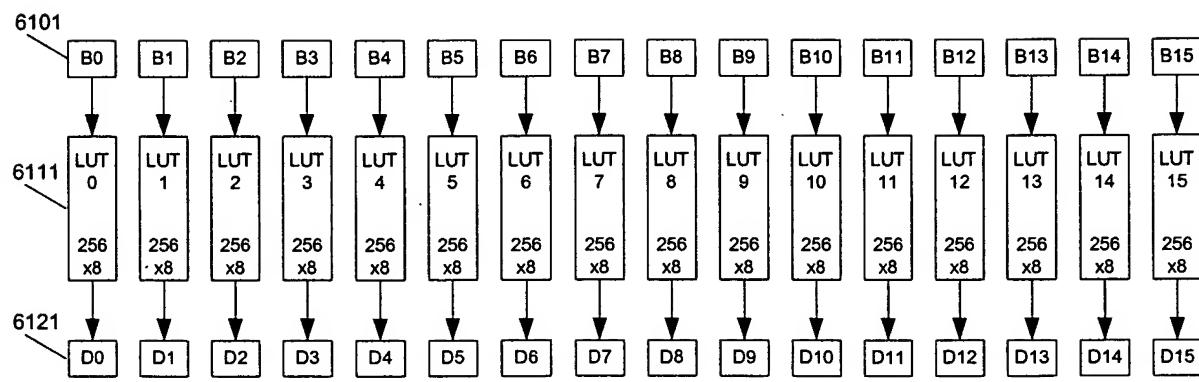


Fig. 41

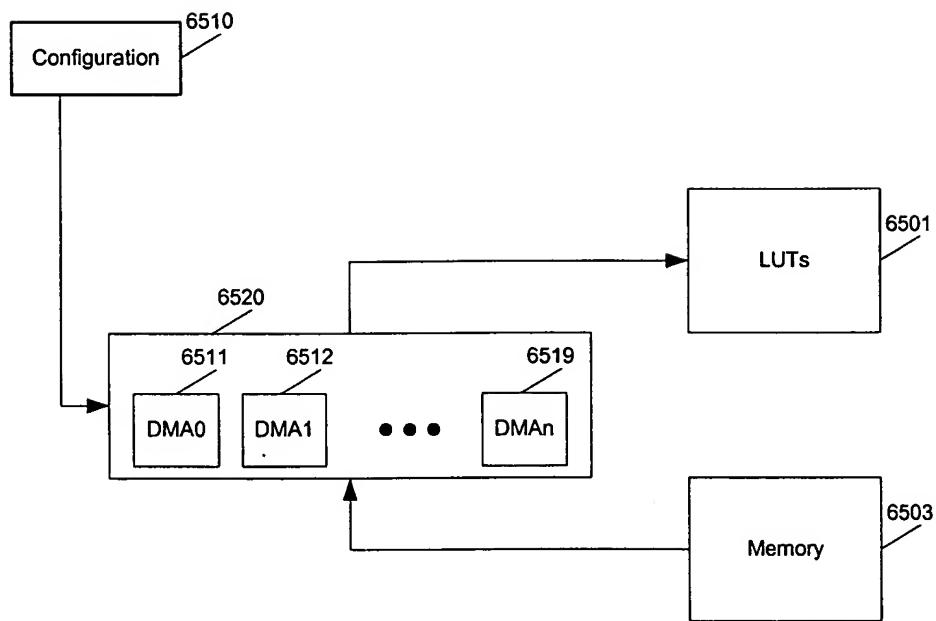


Fig. 45

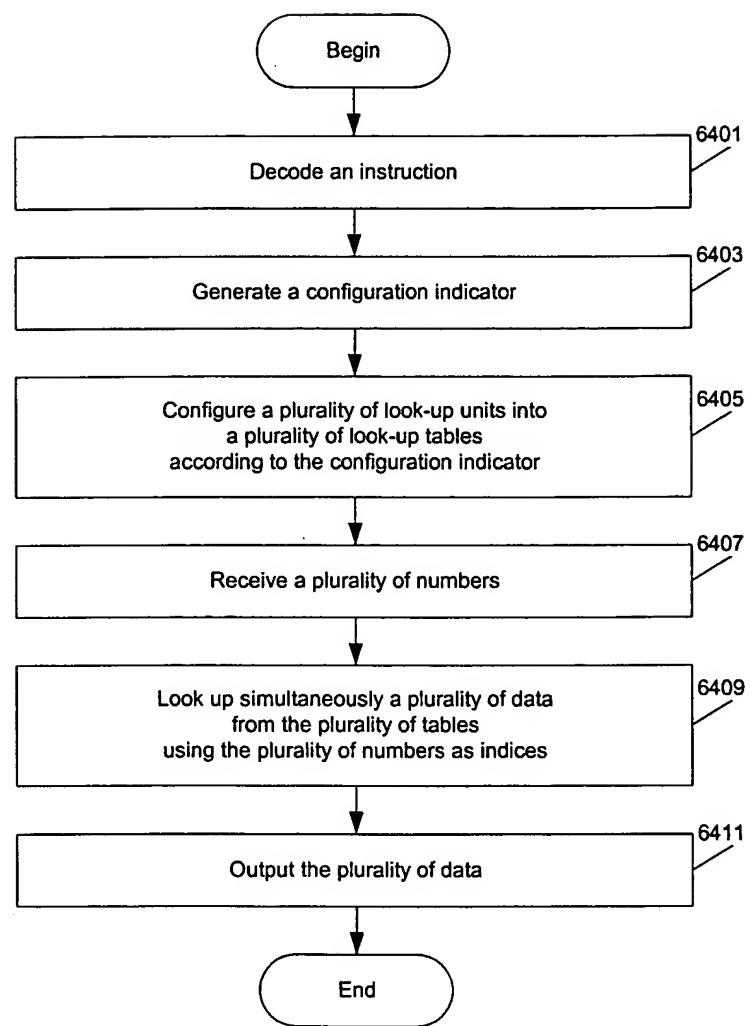


Fig. 44

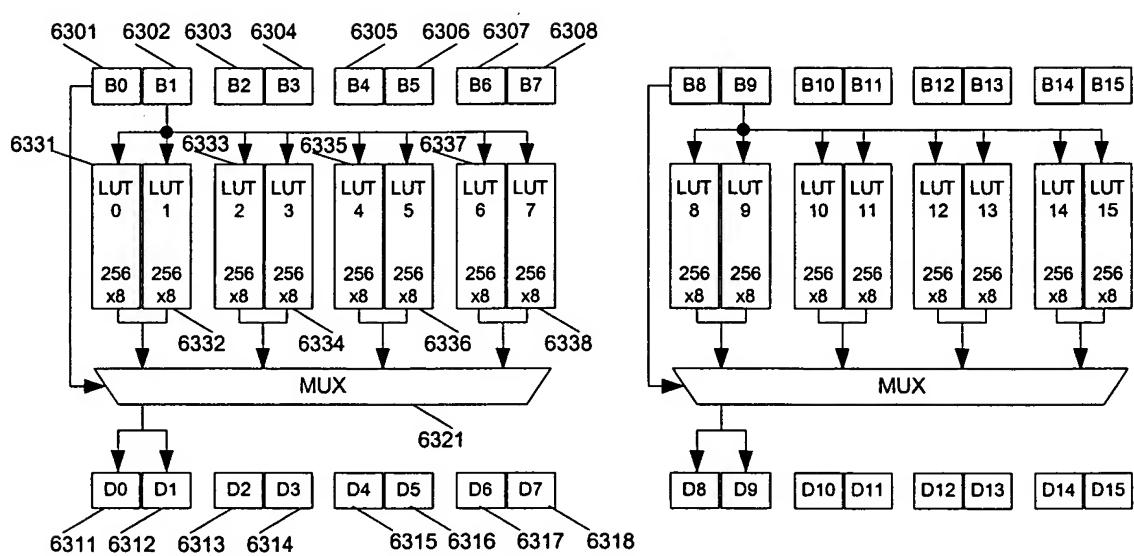


Fig. 43

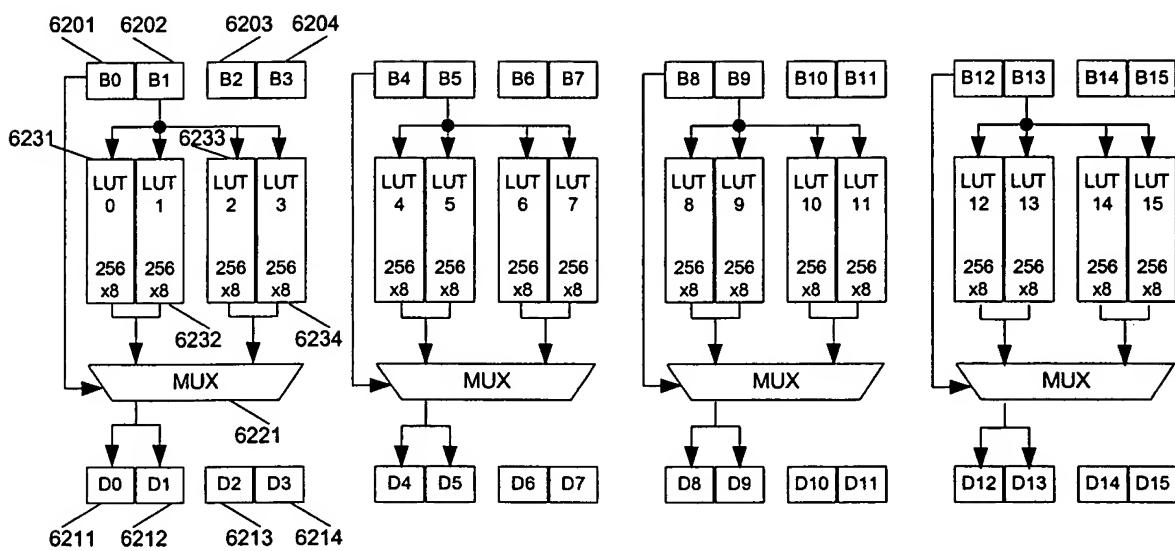


Fig. 42

6610

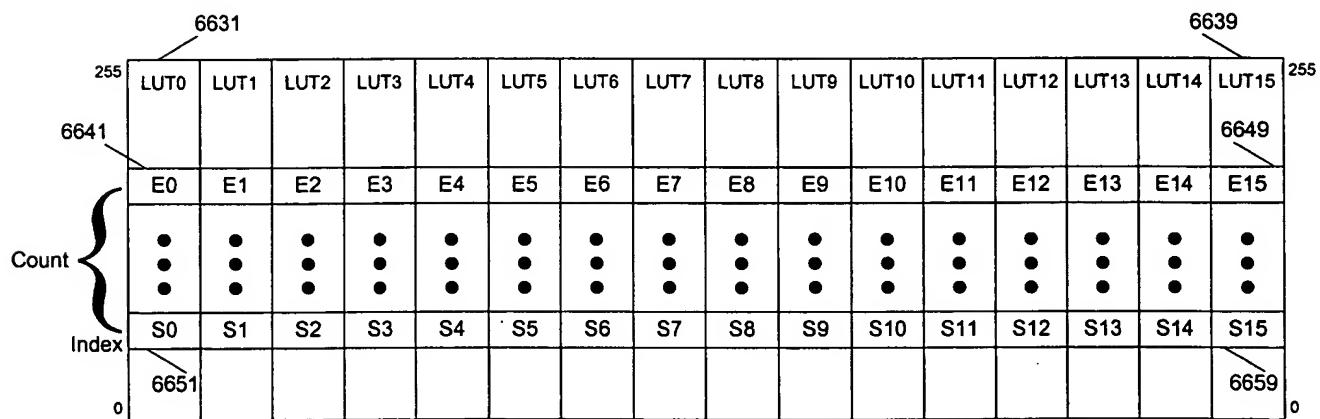
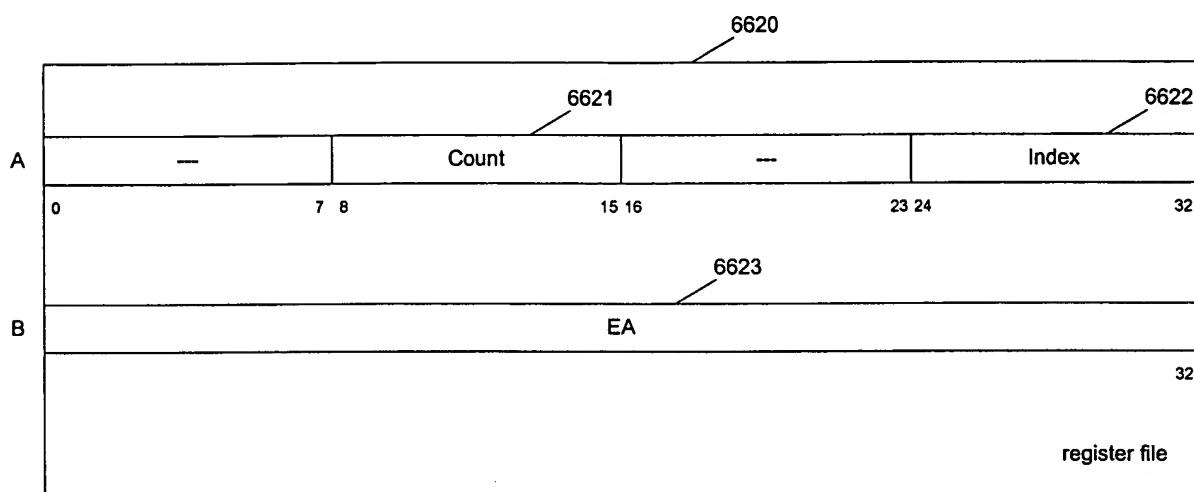
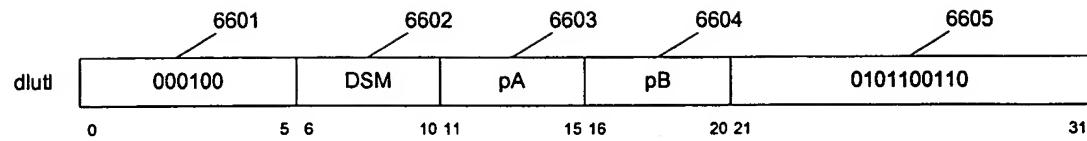


Fig. 46

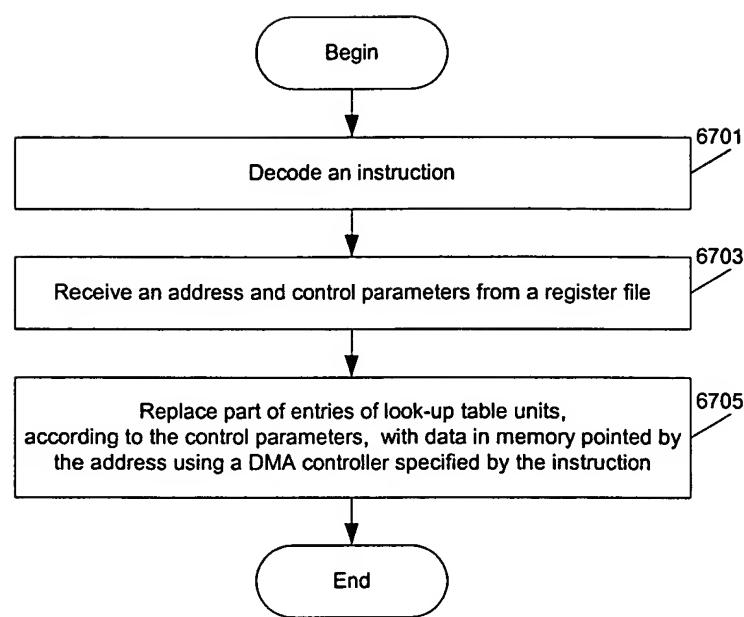


Fig. 47

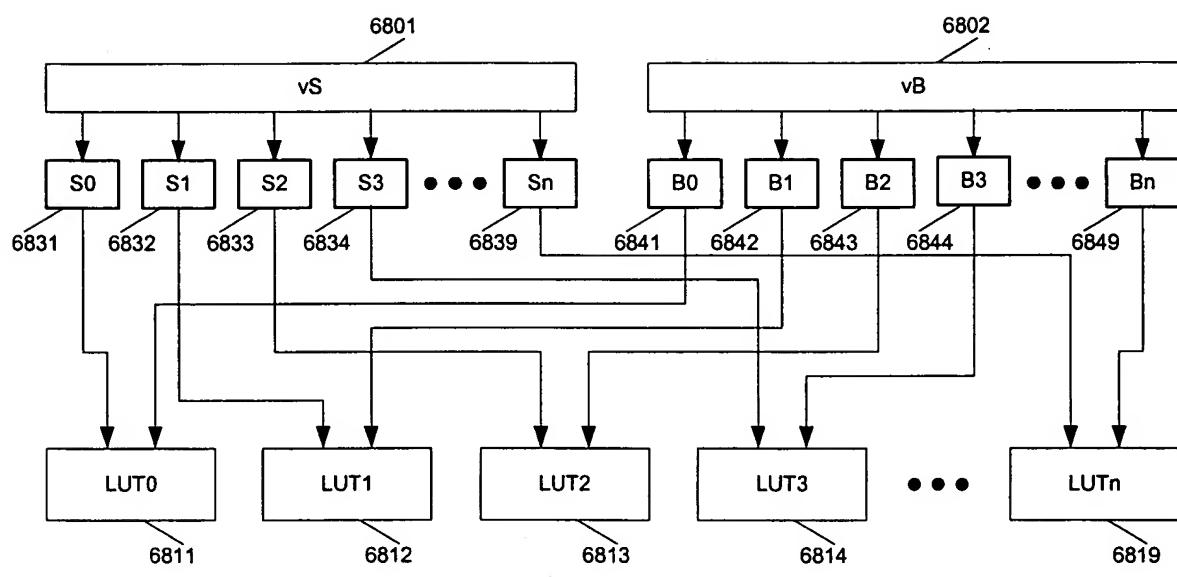


Fig. 48

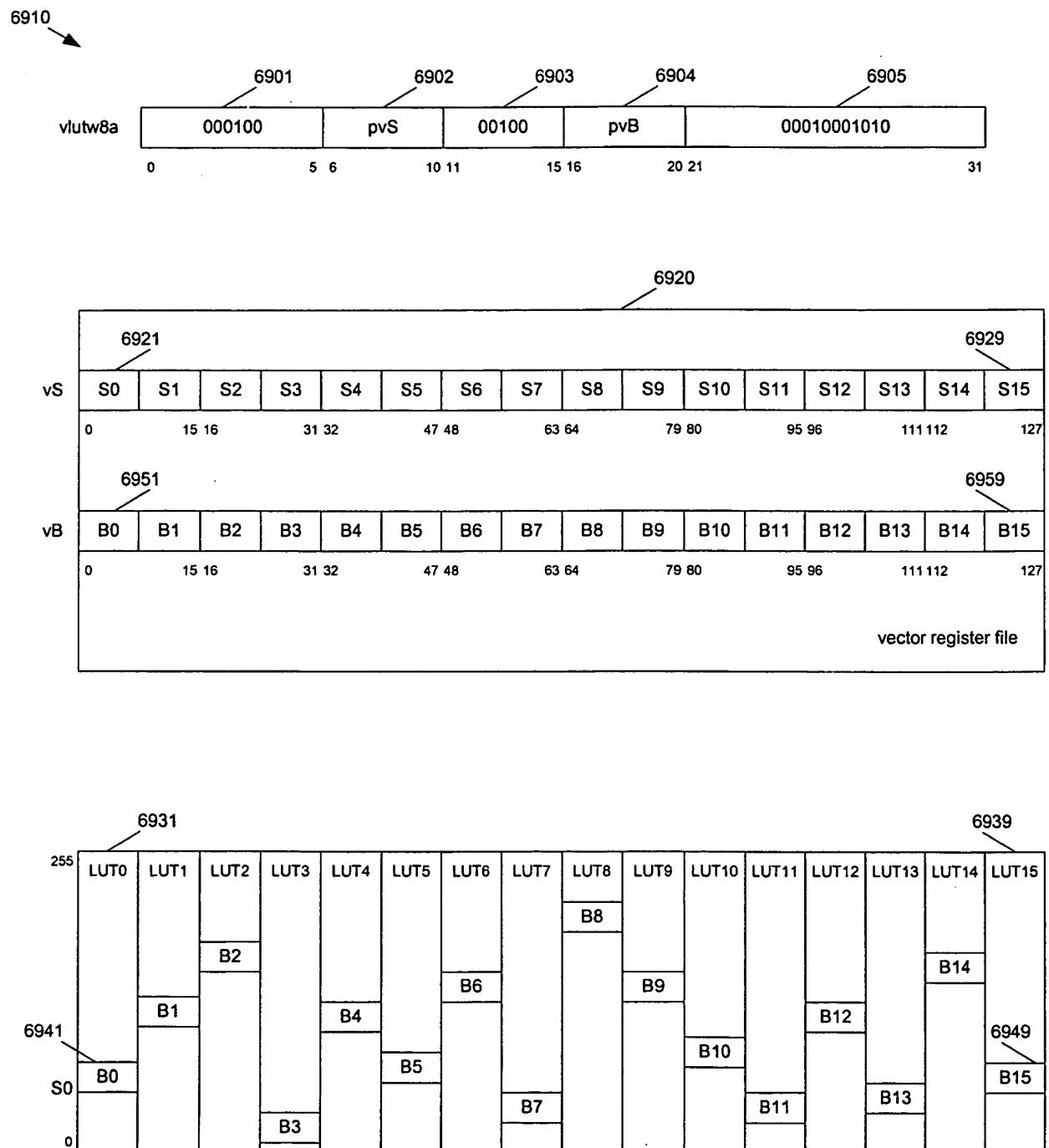


Fig. 49

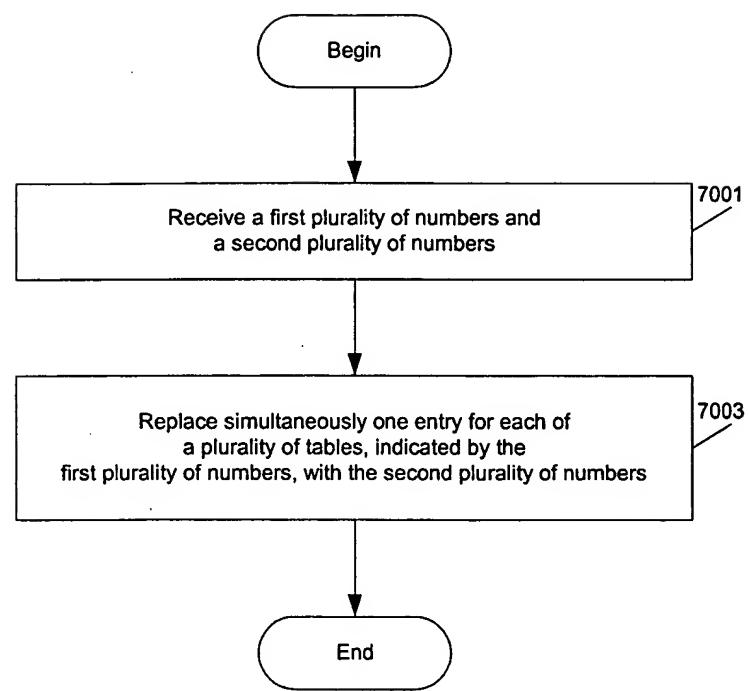


Fig. 50

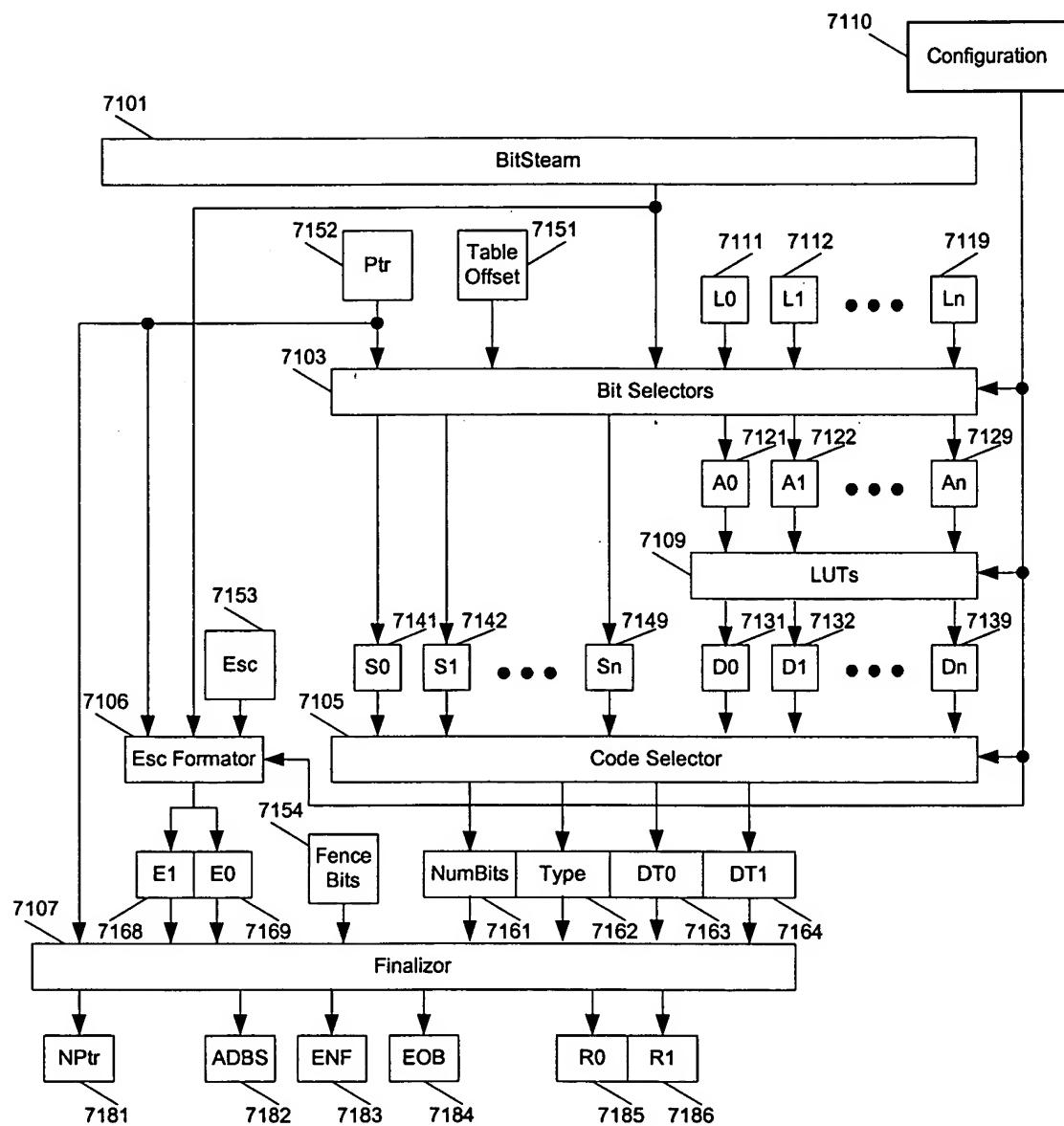


Fig. 51

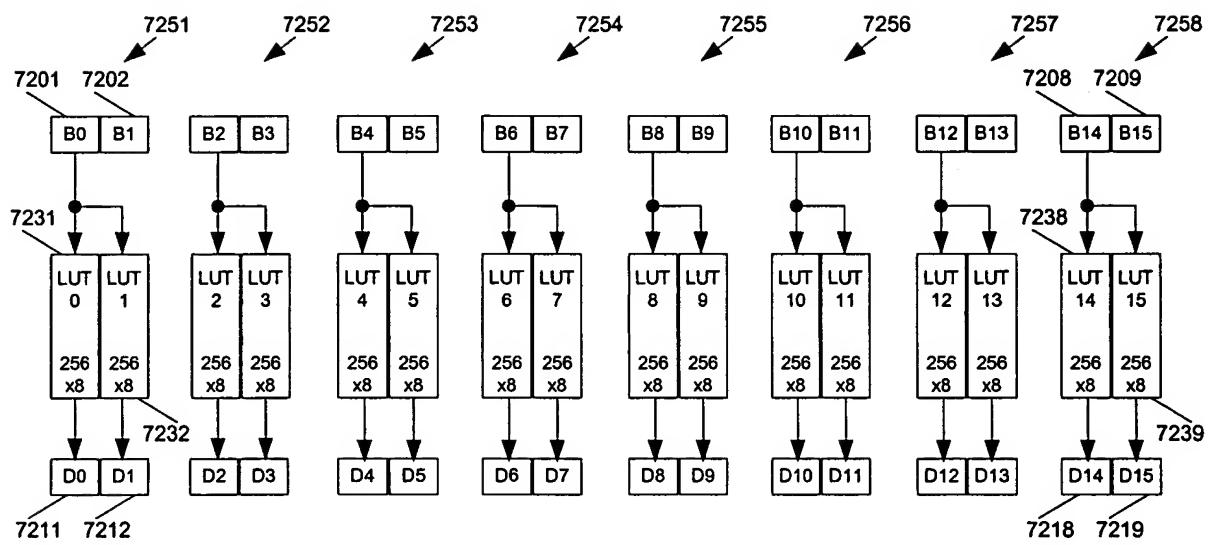


Fig. 52

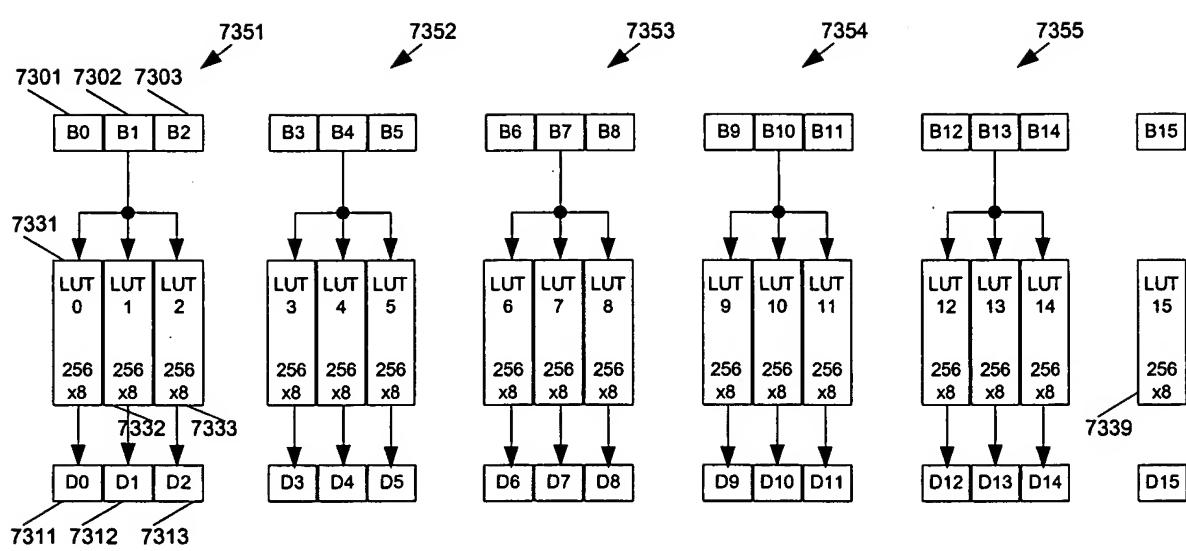


Fig. 53

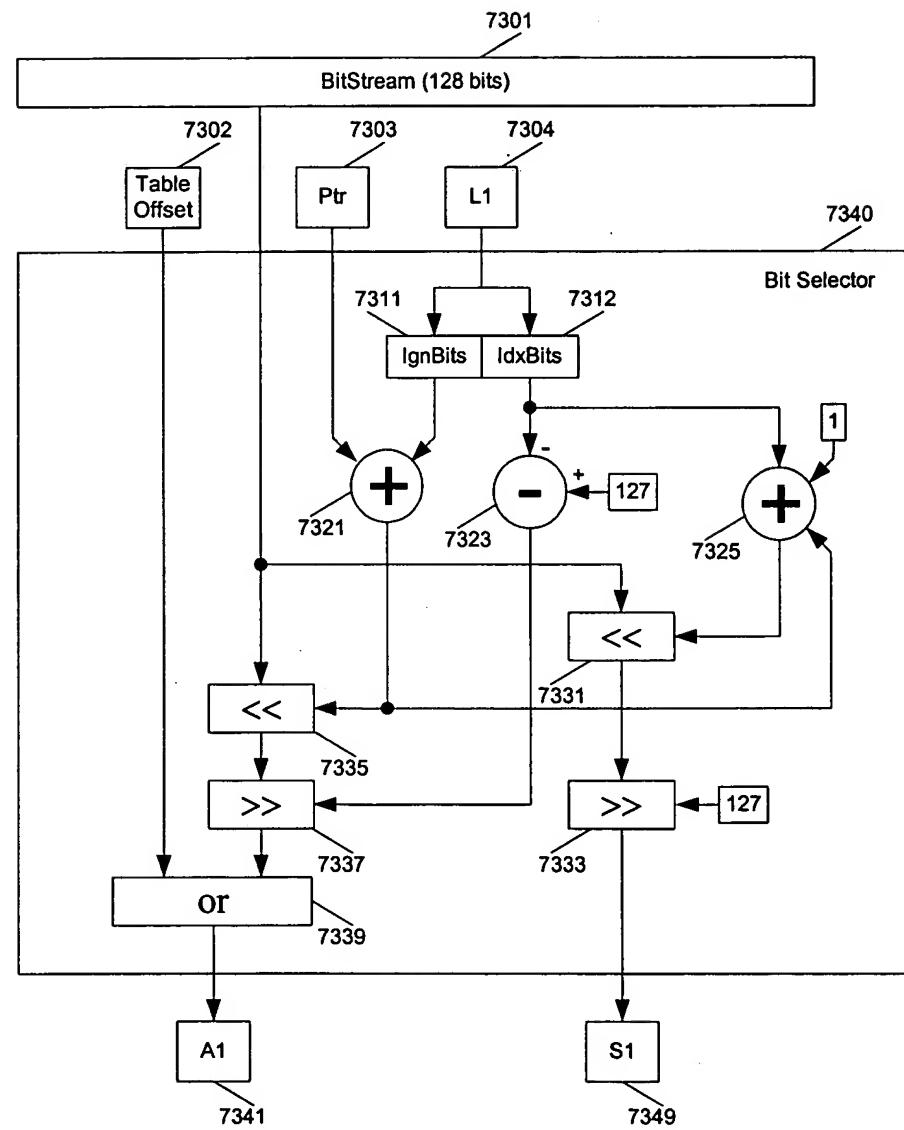


Fig. 54

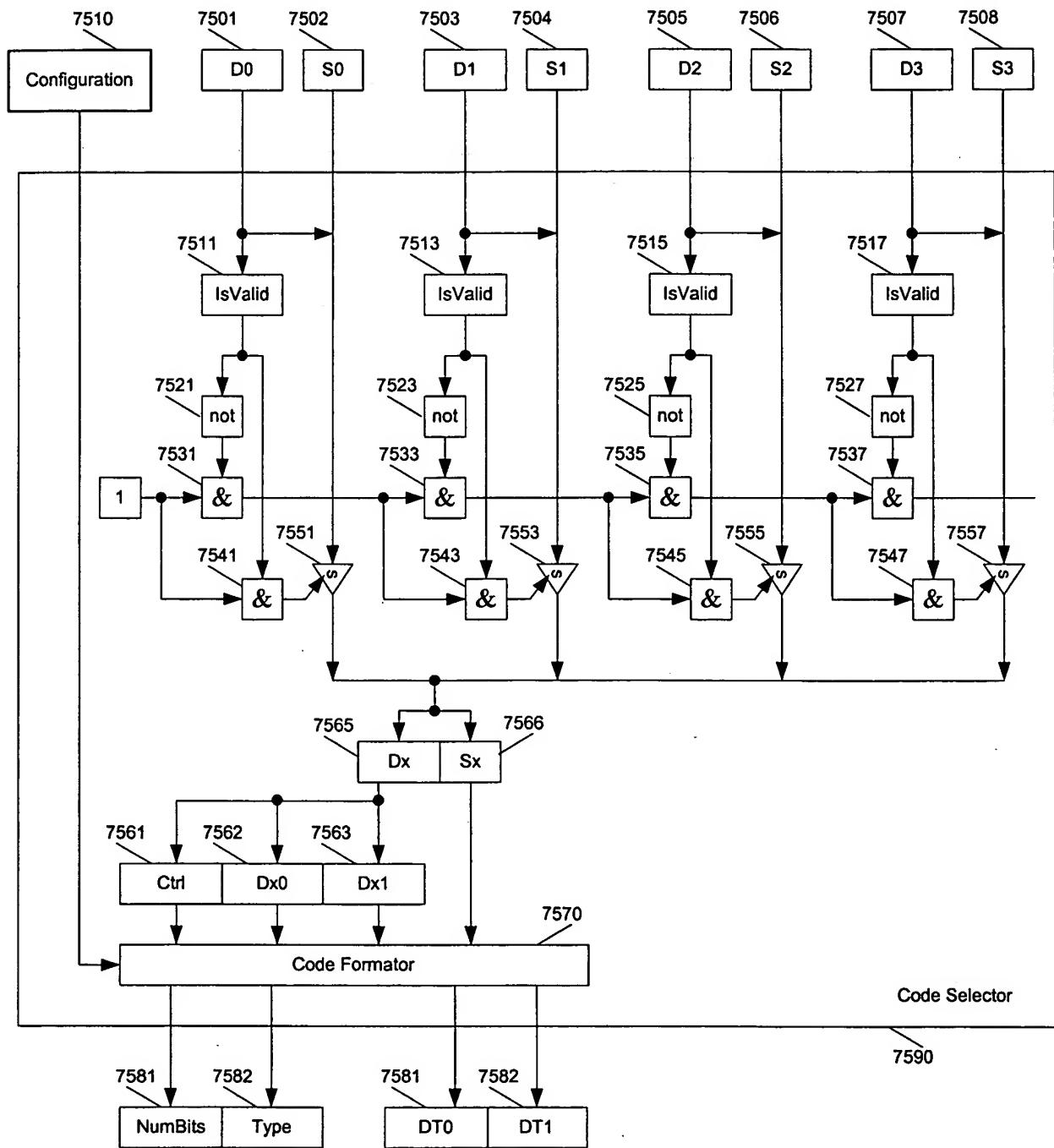


Fig. 55

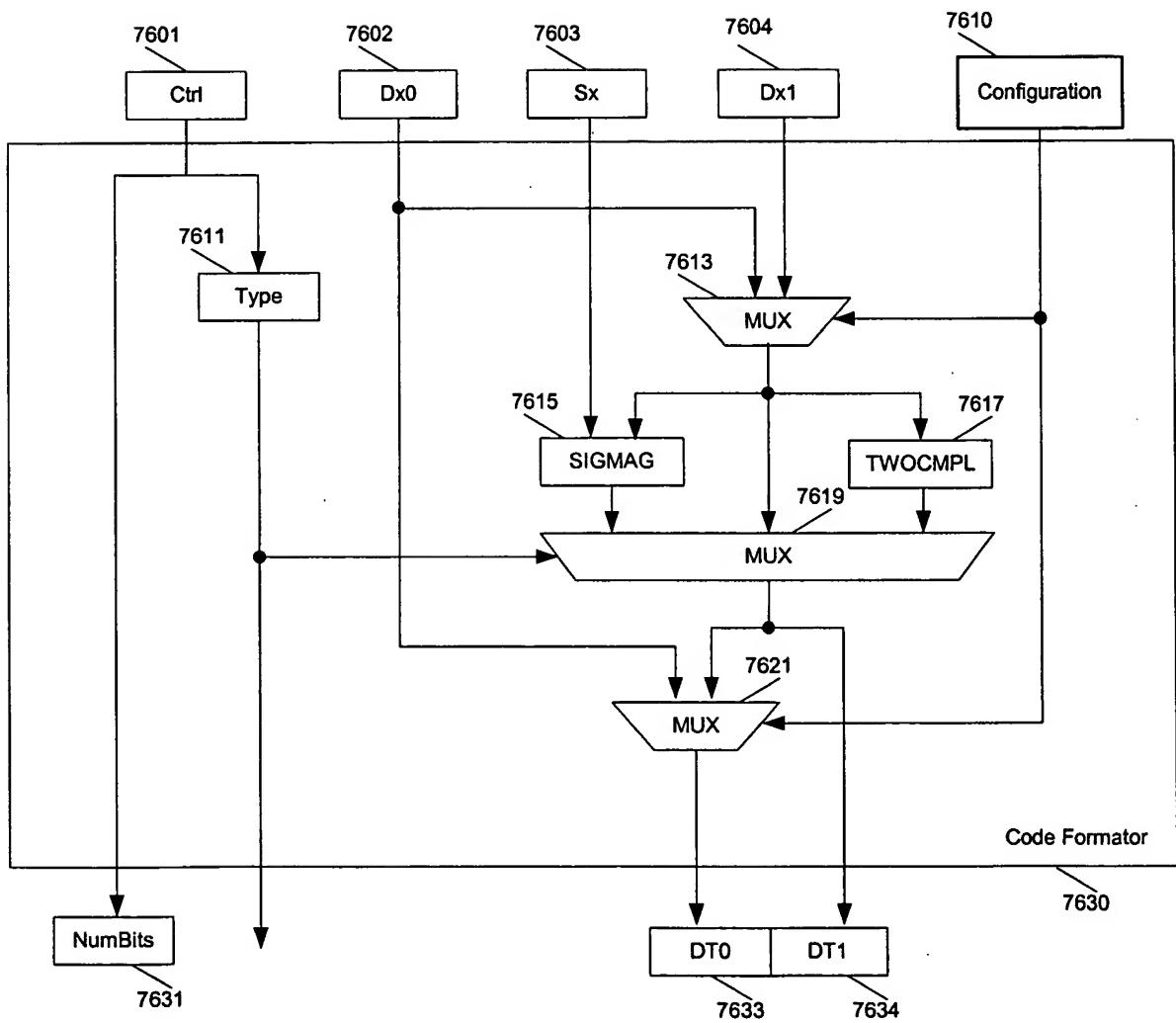


Fig. 56

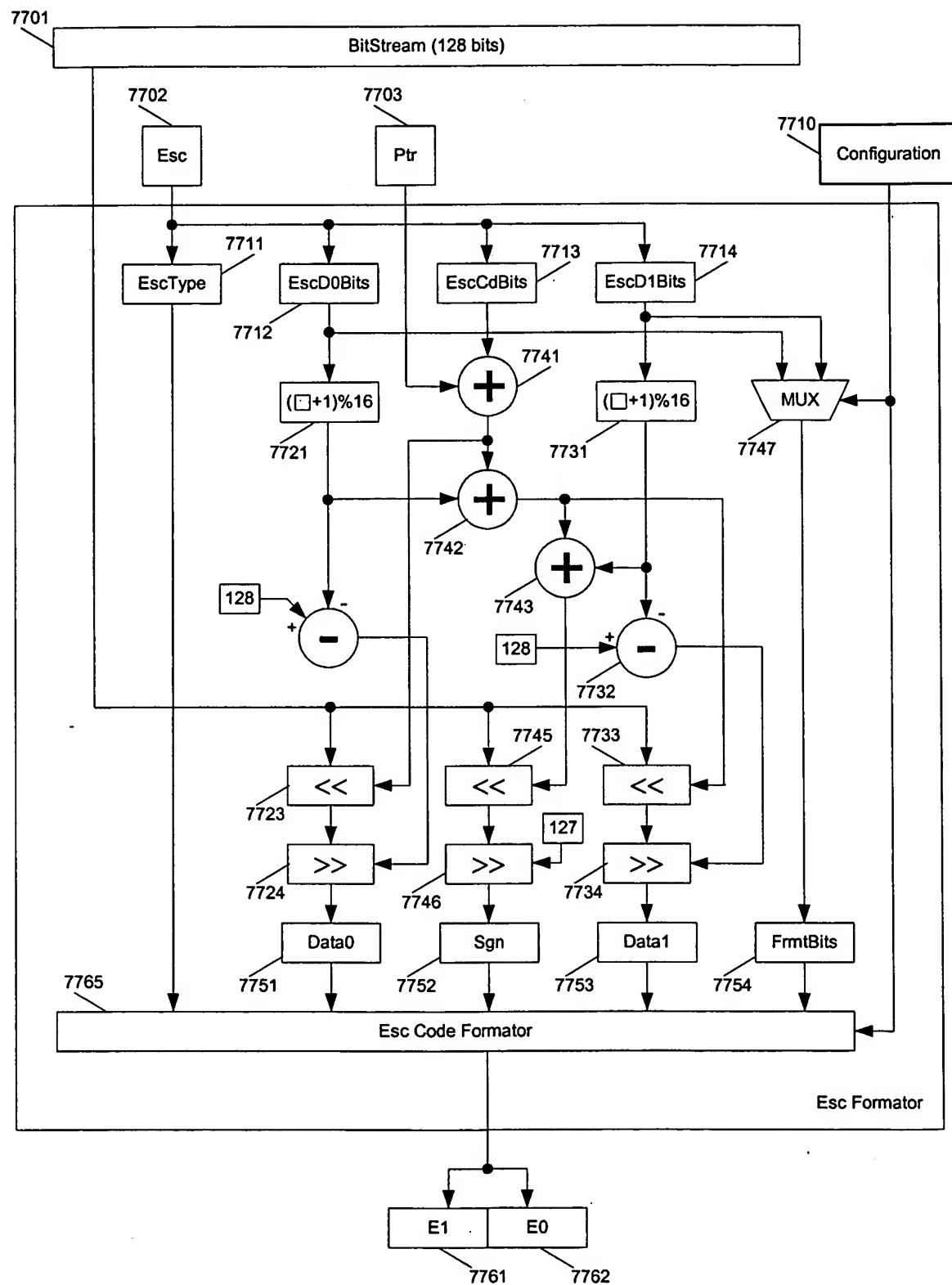


Fig. 57

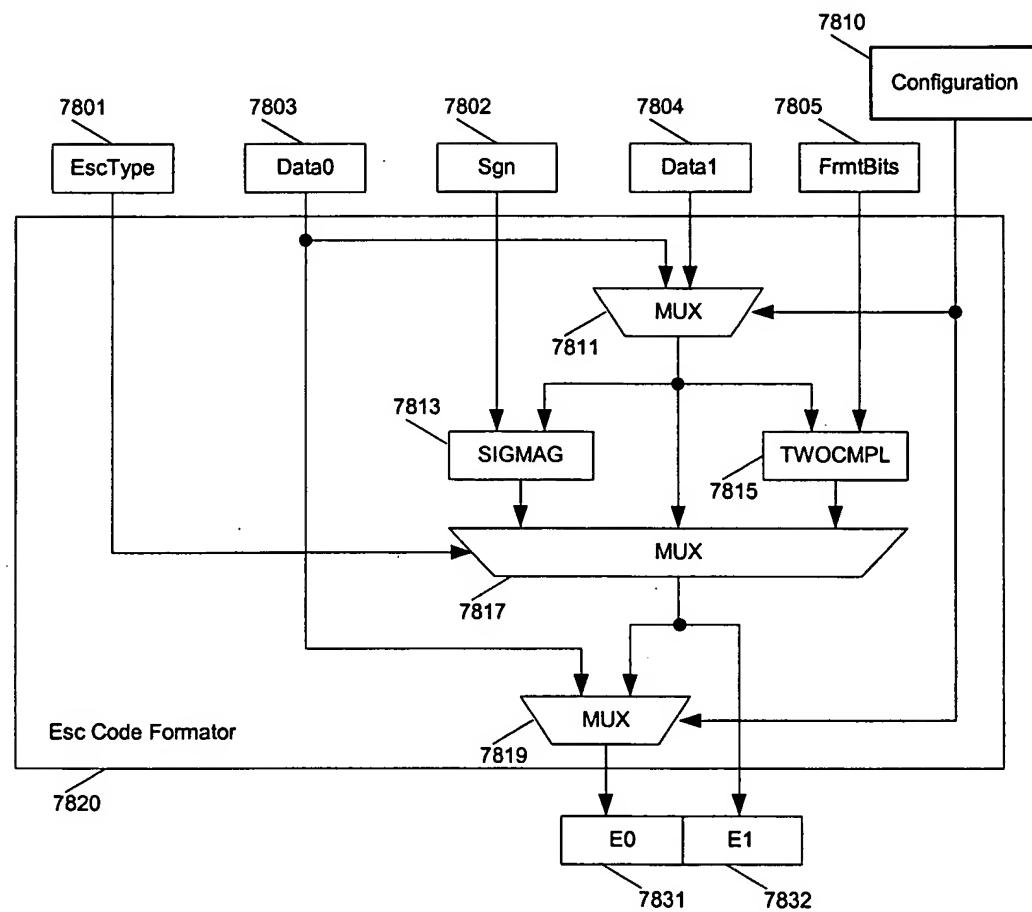


Fig. 58

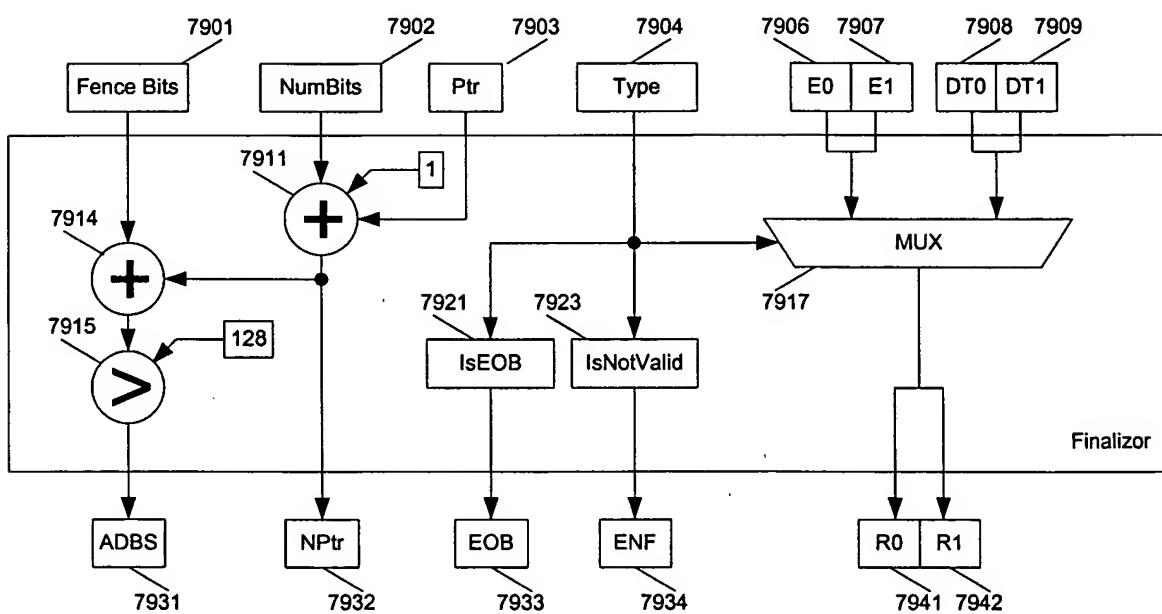


Fig. 59

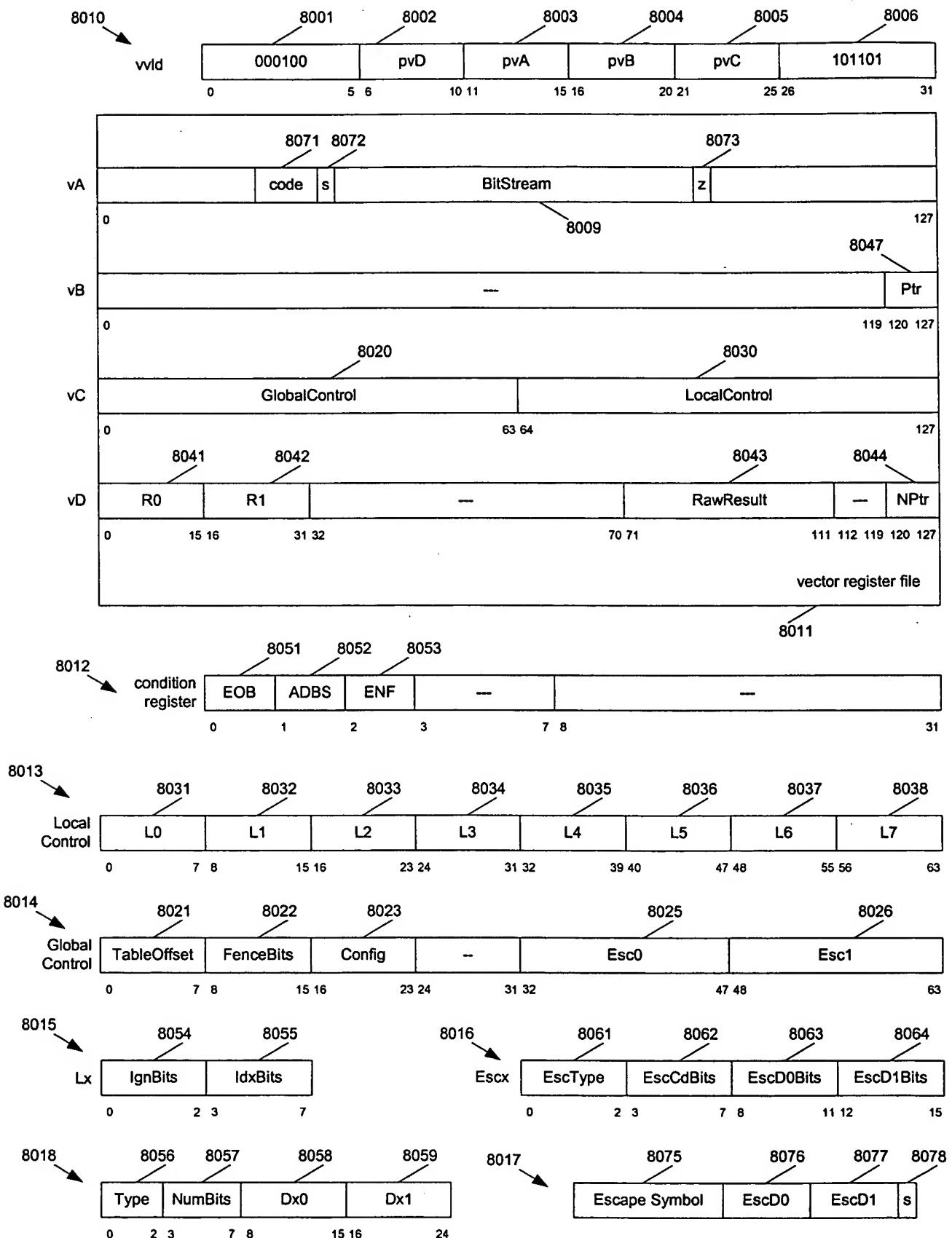


Fig. 60

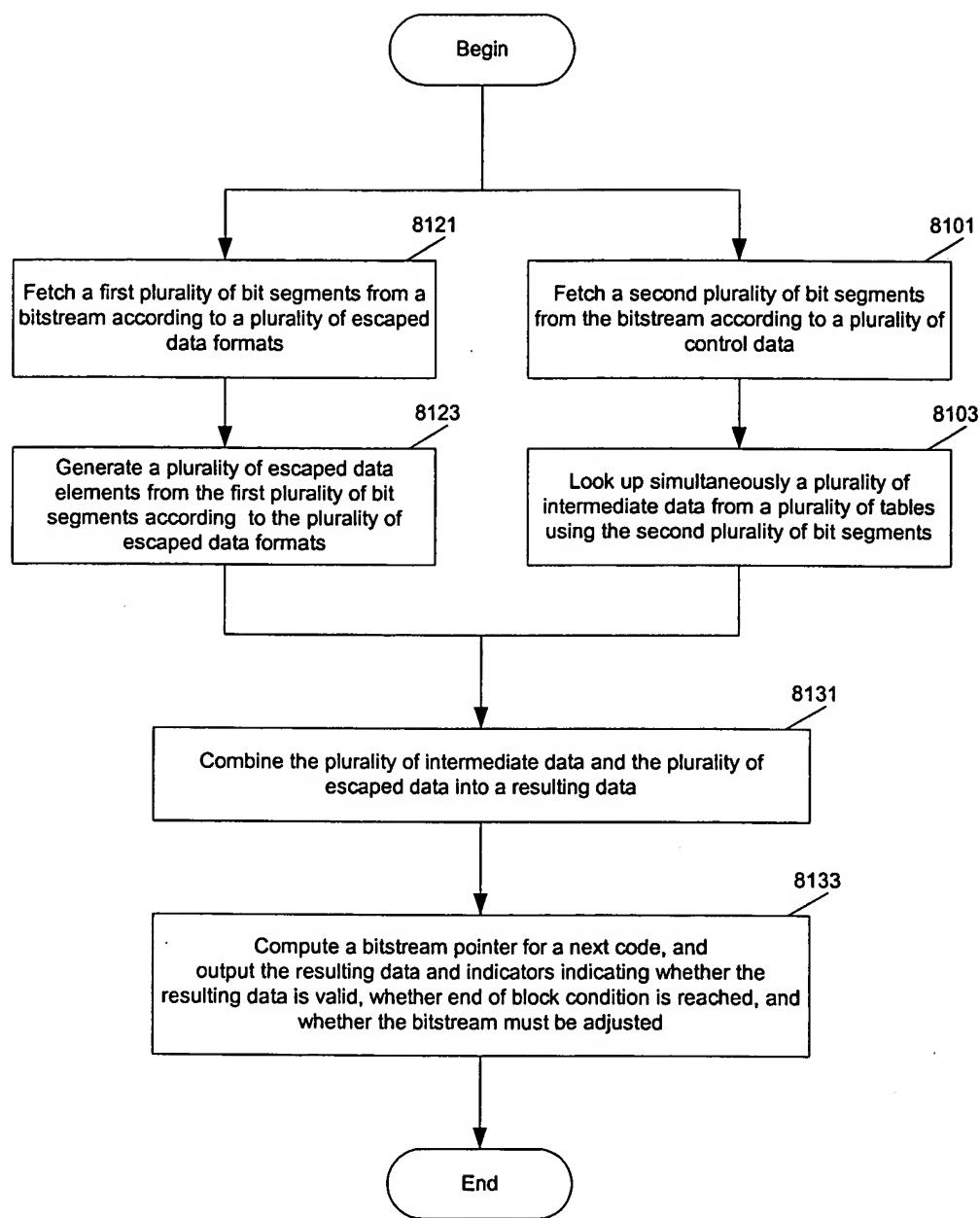


Fig. 61

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	type	bits	run	level												
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02	4	2	0	1	4	6	3	-1	4	9	12	1	4	10	5	-3
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2f	4	5	0	-6	5	8	0	17	0	0	0	0	4	11	5	0
30	0	0	0	0	0	0	0	0	0	0	0	0	5	12	7	2
31	0	0	0	0	0	0	0	0	0	0	0	0	5	12	8	2
32	0	0	0	0	0	0	0	0	0	0	0	0	5	12	9	2
33	0	0	0	0	0	0	0	0	0	0	0	0	5	12	10	2
34	0	0	0	0	0	0	0	0	0	0	0	0	5	12	7	3
35	0	0	0	0	0	0	0	0	0	0	0	0	5	12	8	3
36	0	0	0	0	0	0	0	0	0	0	0	0	5	12	4	5
37	0	0	0	0	0	0	0	0	0	0	0	0	5	12	3	7
38	0	0	0	0	0	0	0	0	0	0	0	0	5	12	2	7
39	0	0	0	0	0	0	0	0	0	0	0	0	5	12	2	8
3a	0	0	0	0	0	0	0	0	0	0	0	0	5	12	2	9
3b	0	0	0	0	0	0	0	0	0	0	0	0	5	12	2	10
3c	0	0	0	0	2	12	0	0	0	0	0	0	5	12	2	11
3d	0	0	0	0	2	12	0	0	0	0	0	0	5	12	1	15
3e	0	0	0	0	3	15	0	0	0	0	0	0	5	12	1	16
3f	0	0	0	0	3	15	0	0	0	0	0	0	5	12	1	17
40	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
...	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ff	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fig. 62

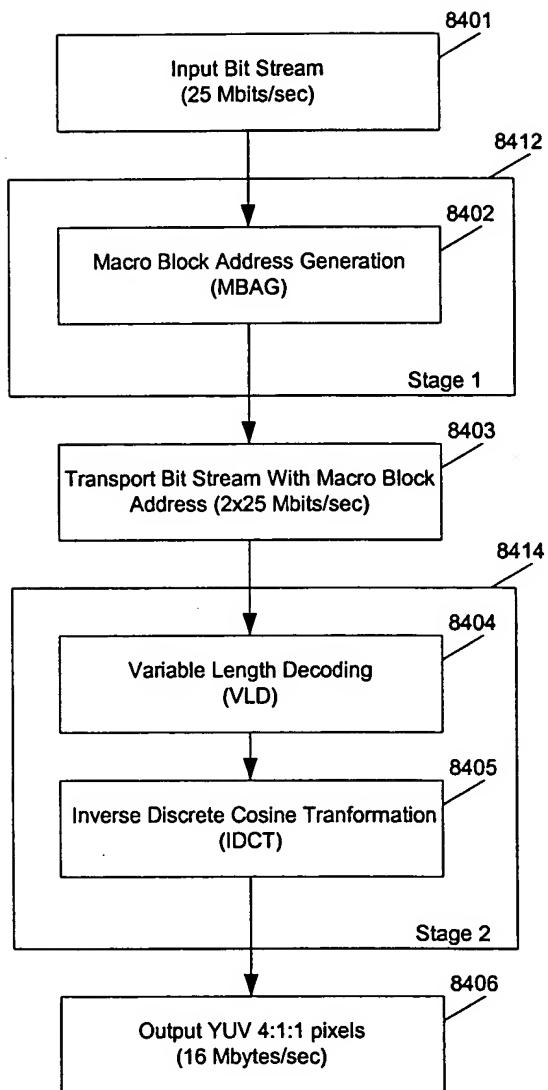


Fig. 64

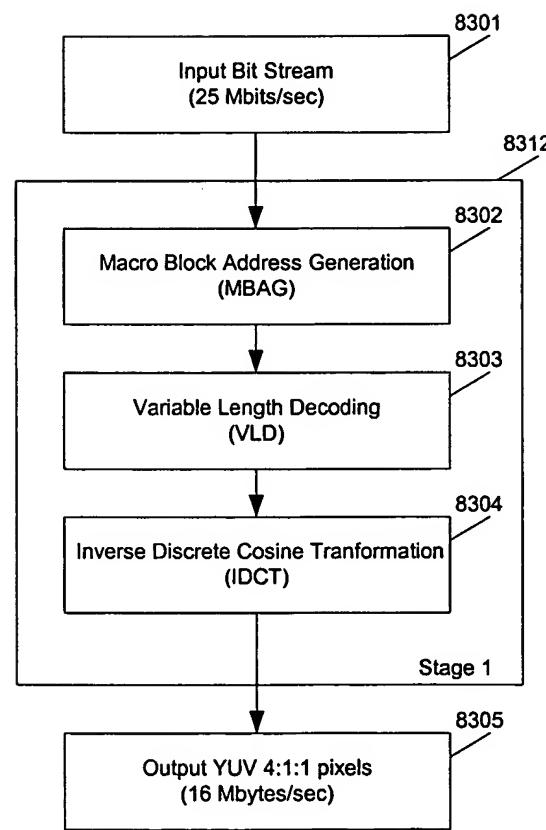


Fig. 63

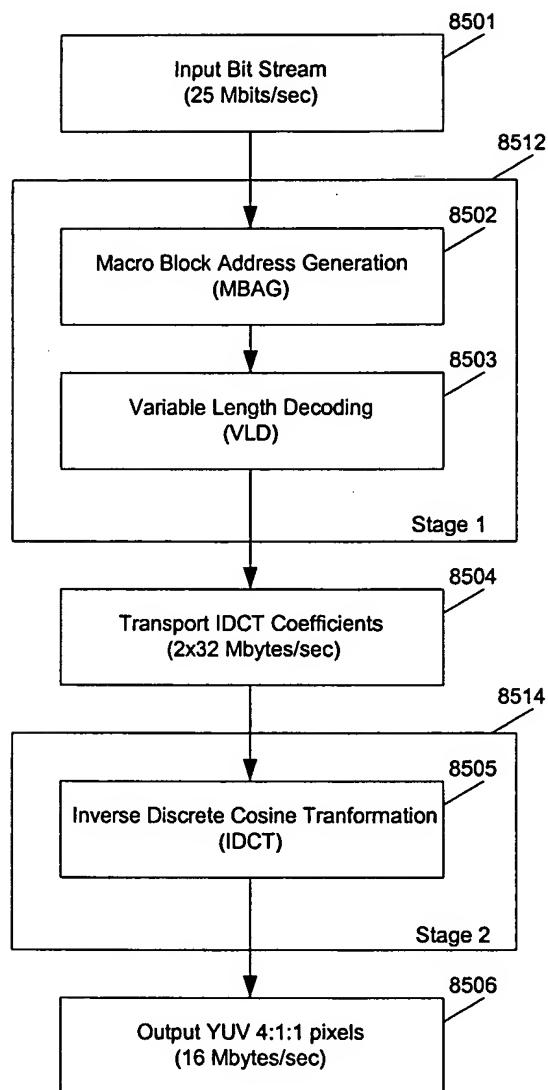


Fig. 65

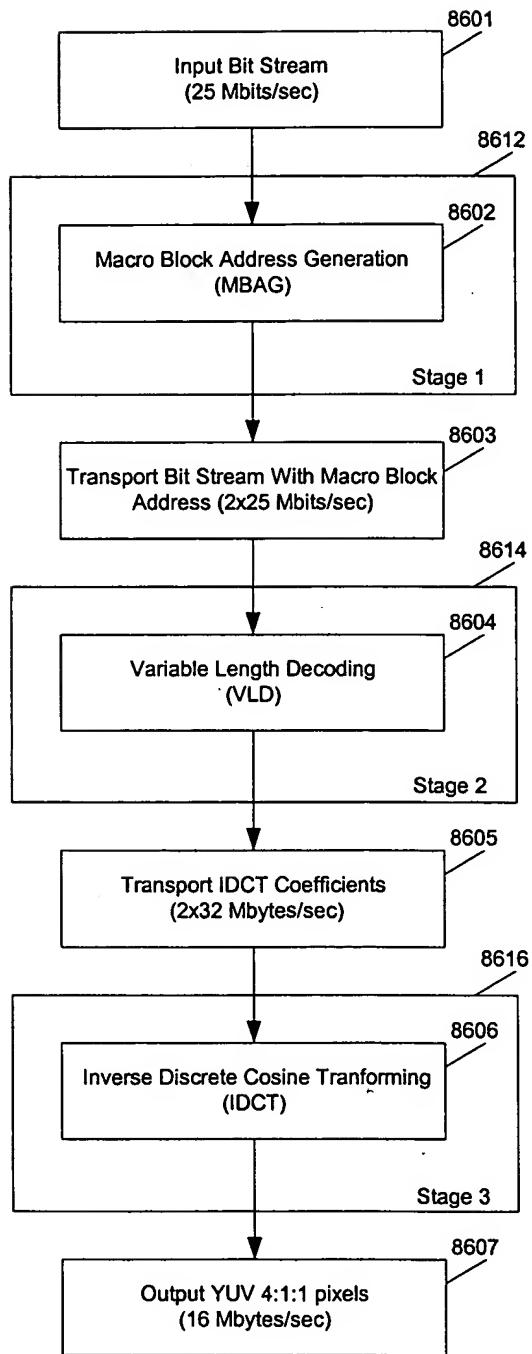


Fig. 66

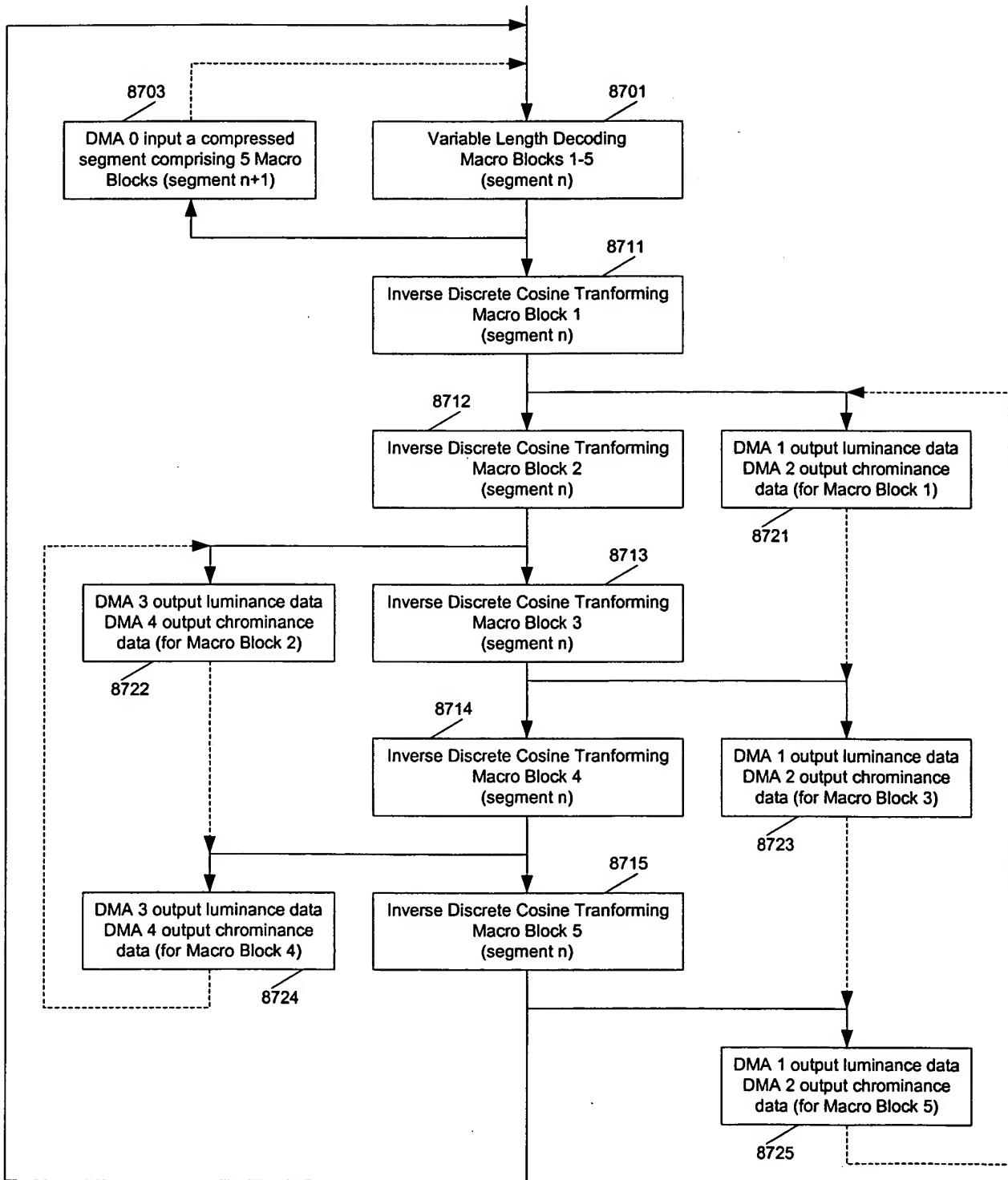


Fig. 67

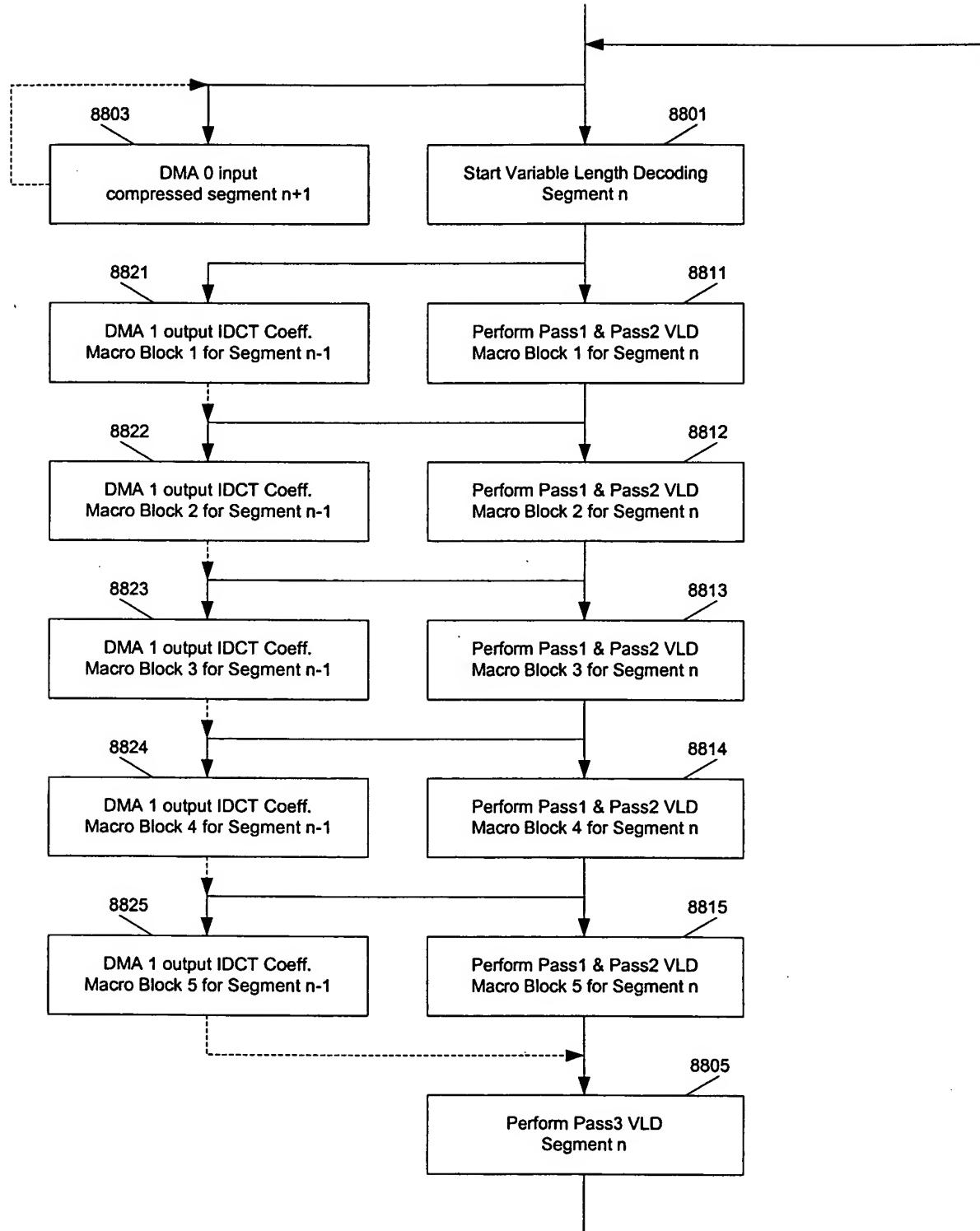


Fig. 68

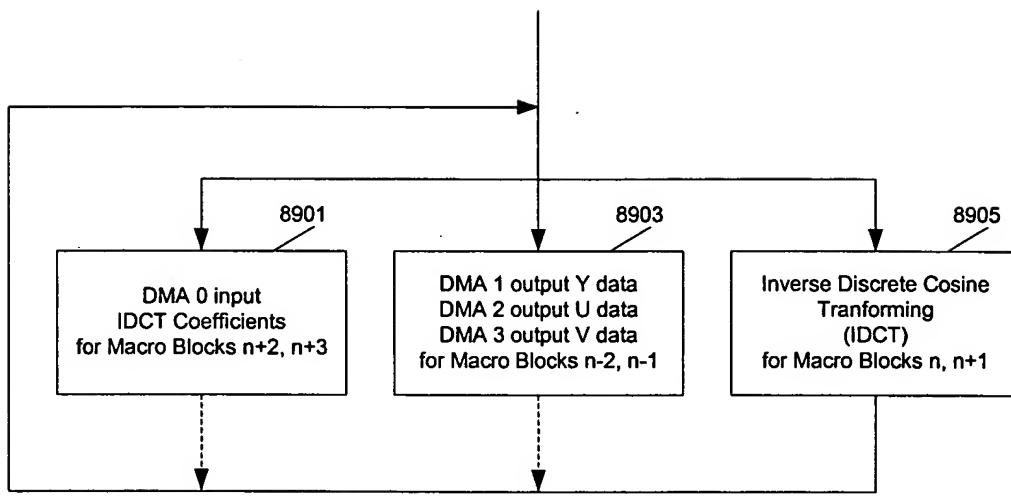


Fig. 69

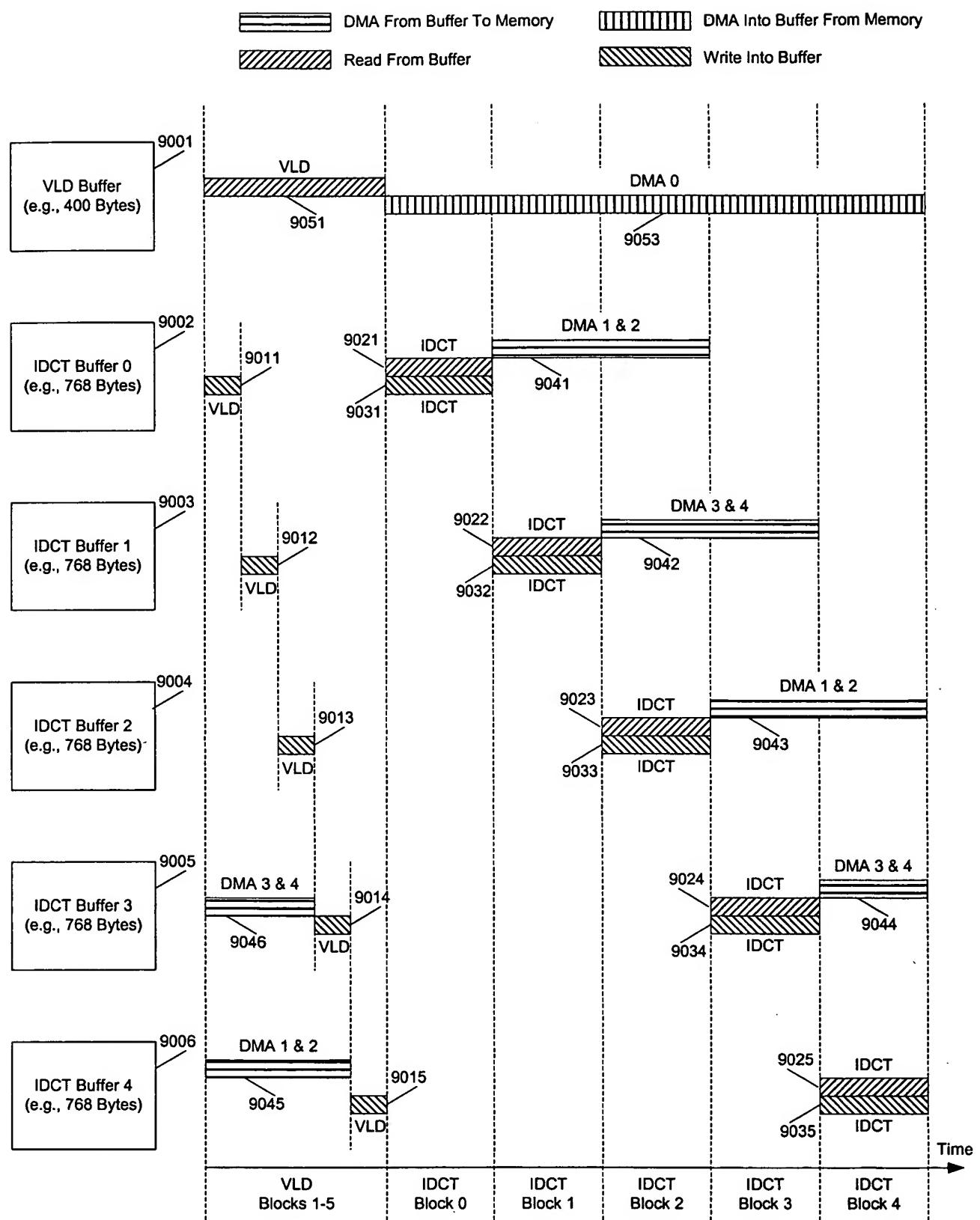


Fig. 70

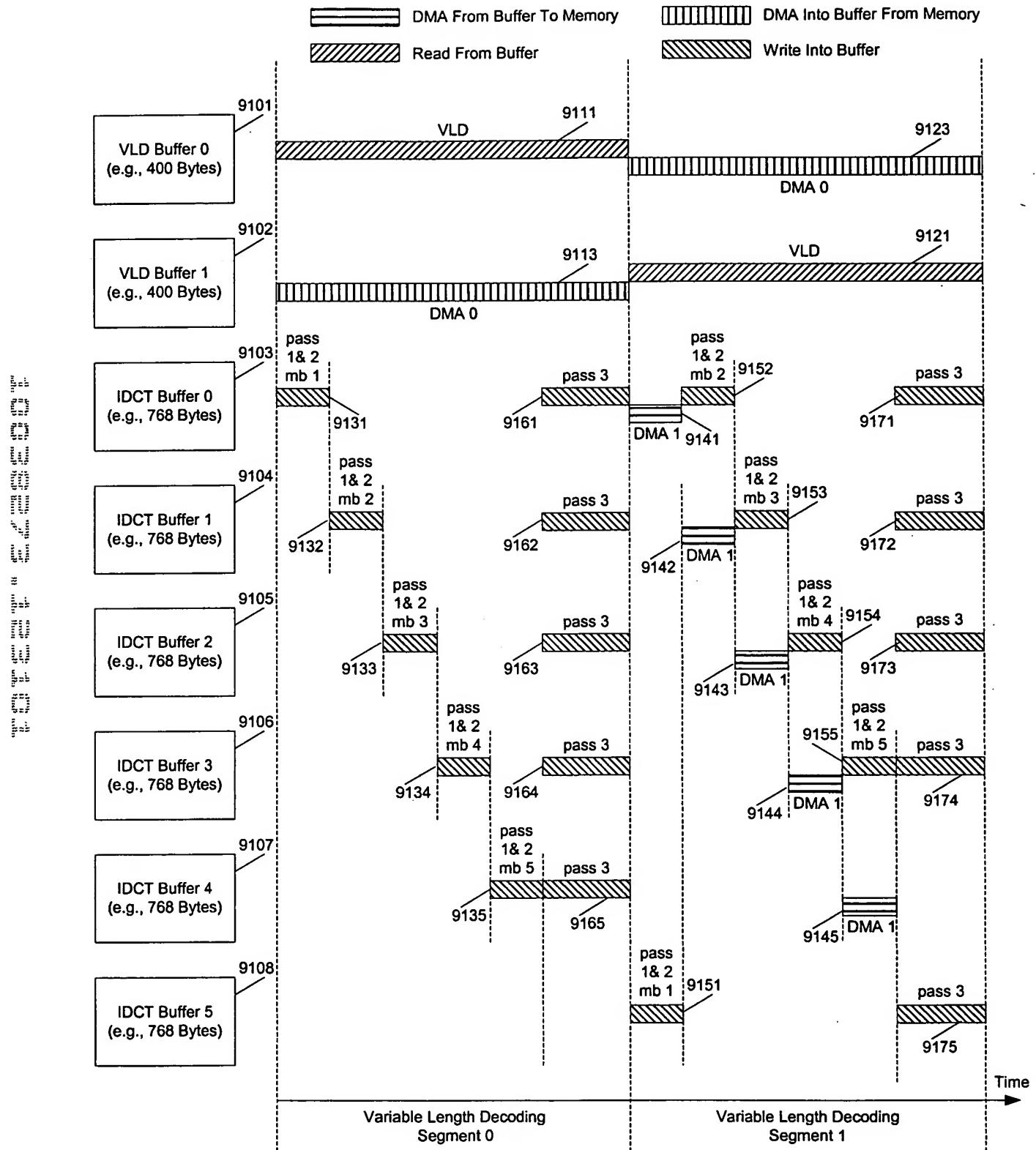


Fig. 71

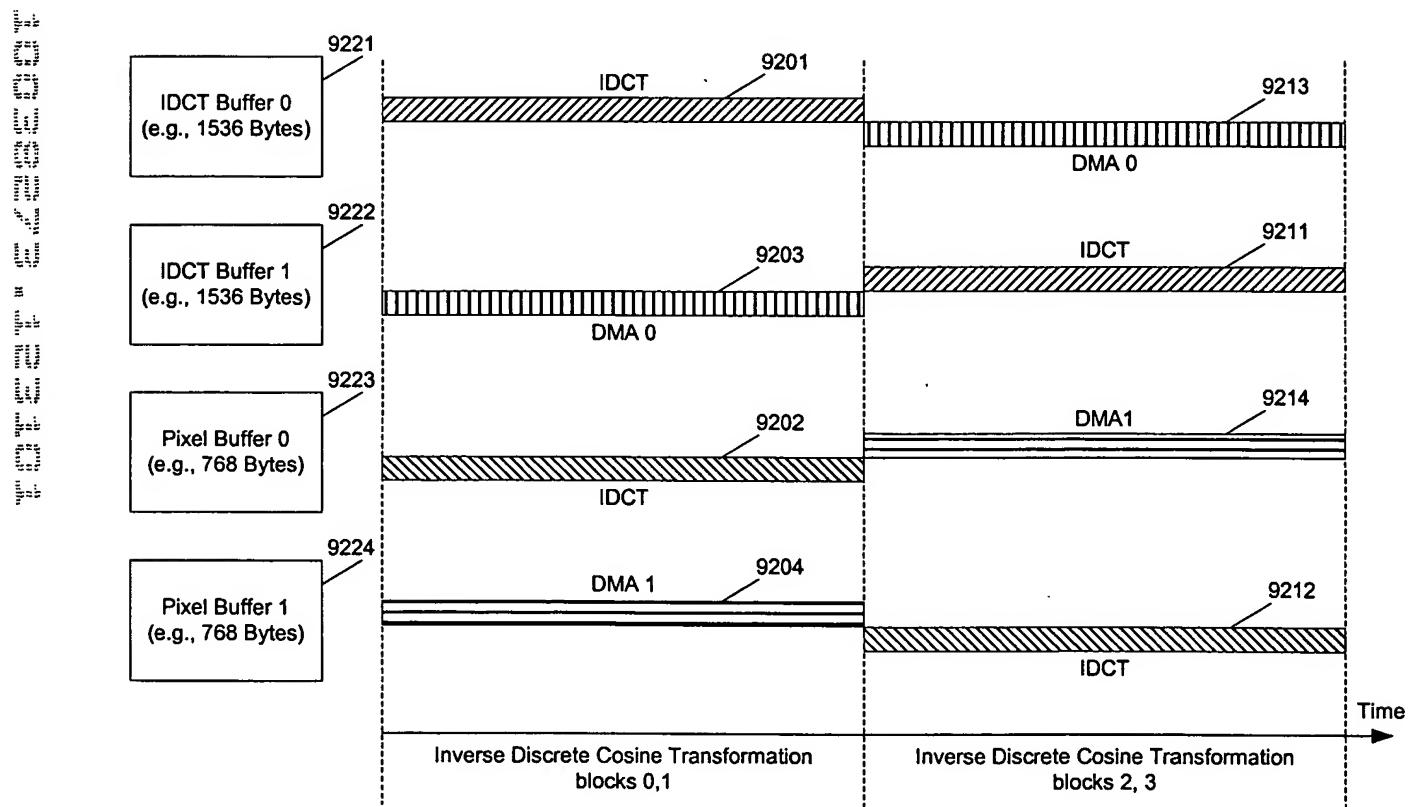


Fig. 72

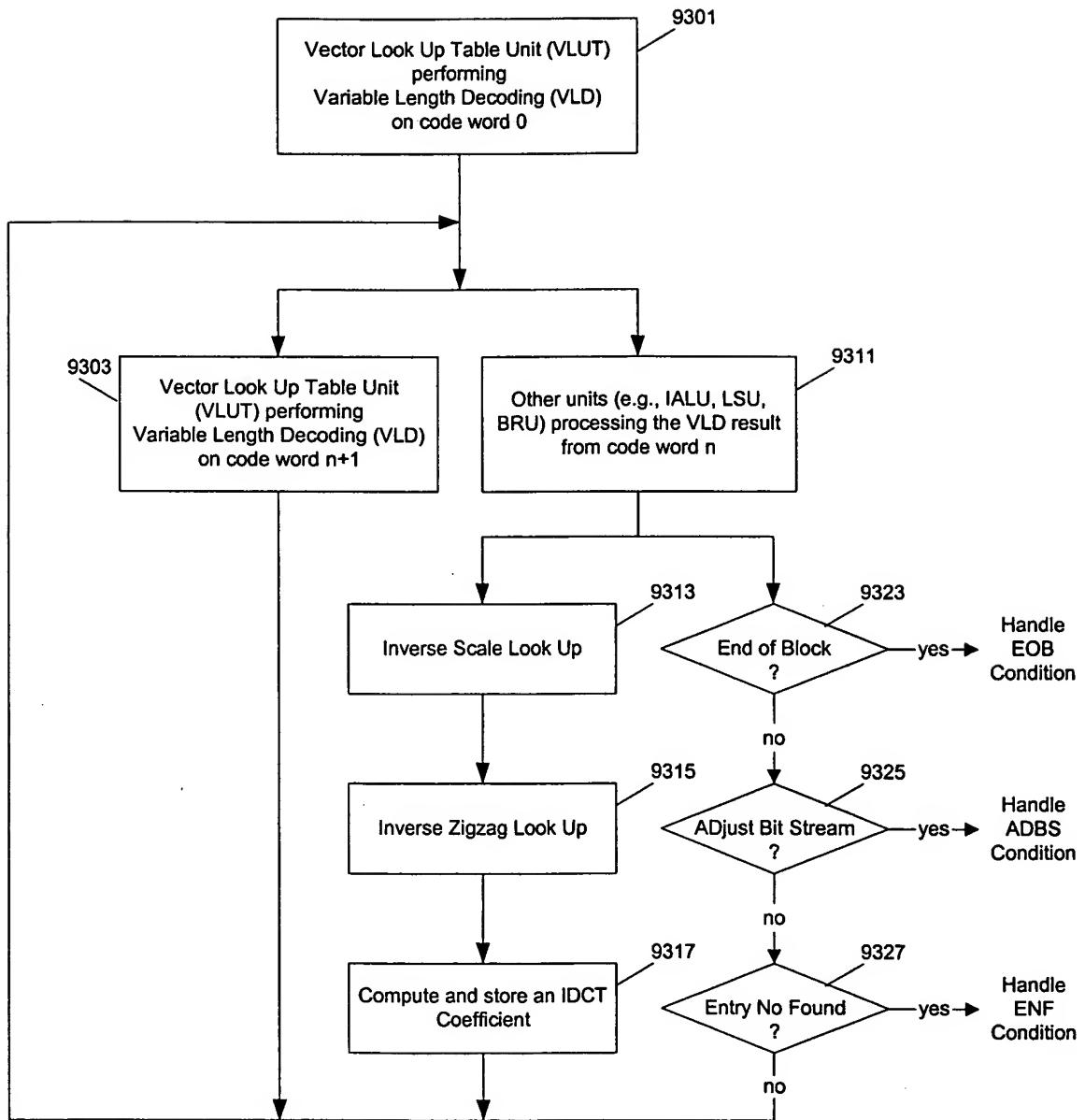


Fig. 73

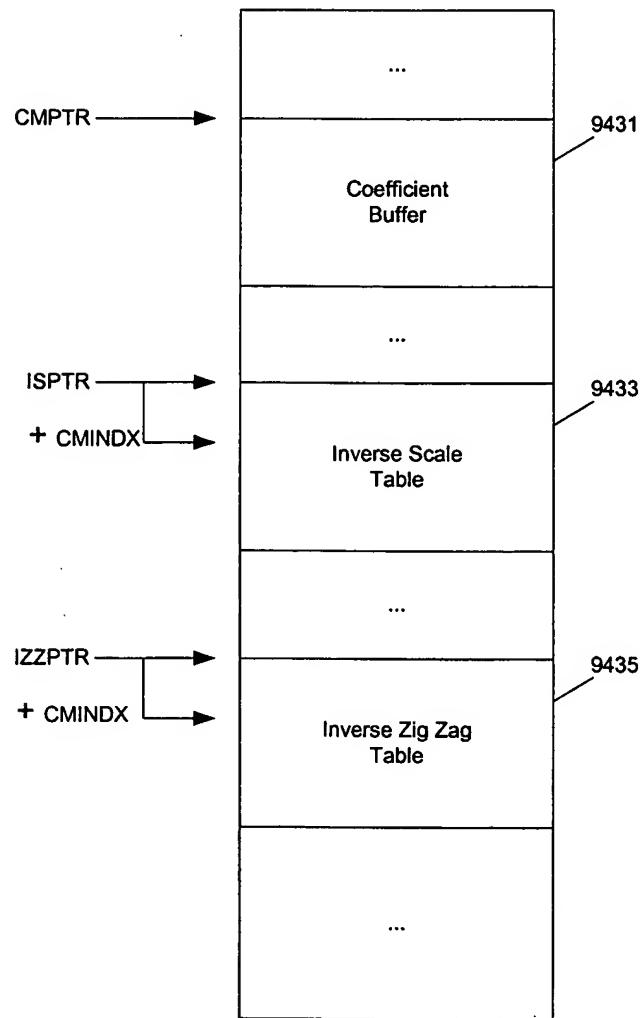
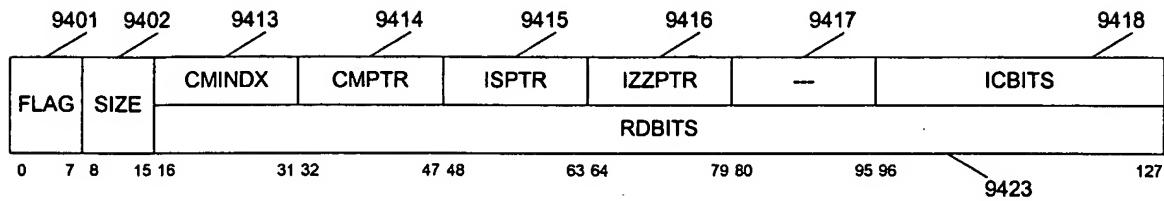


Fig. 74

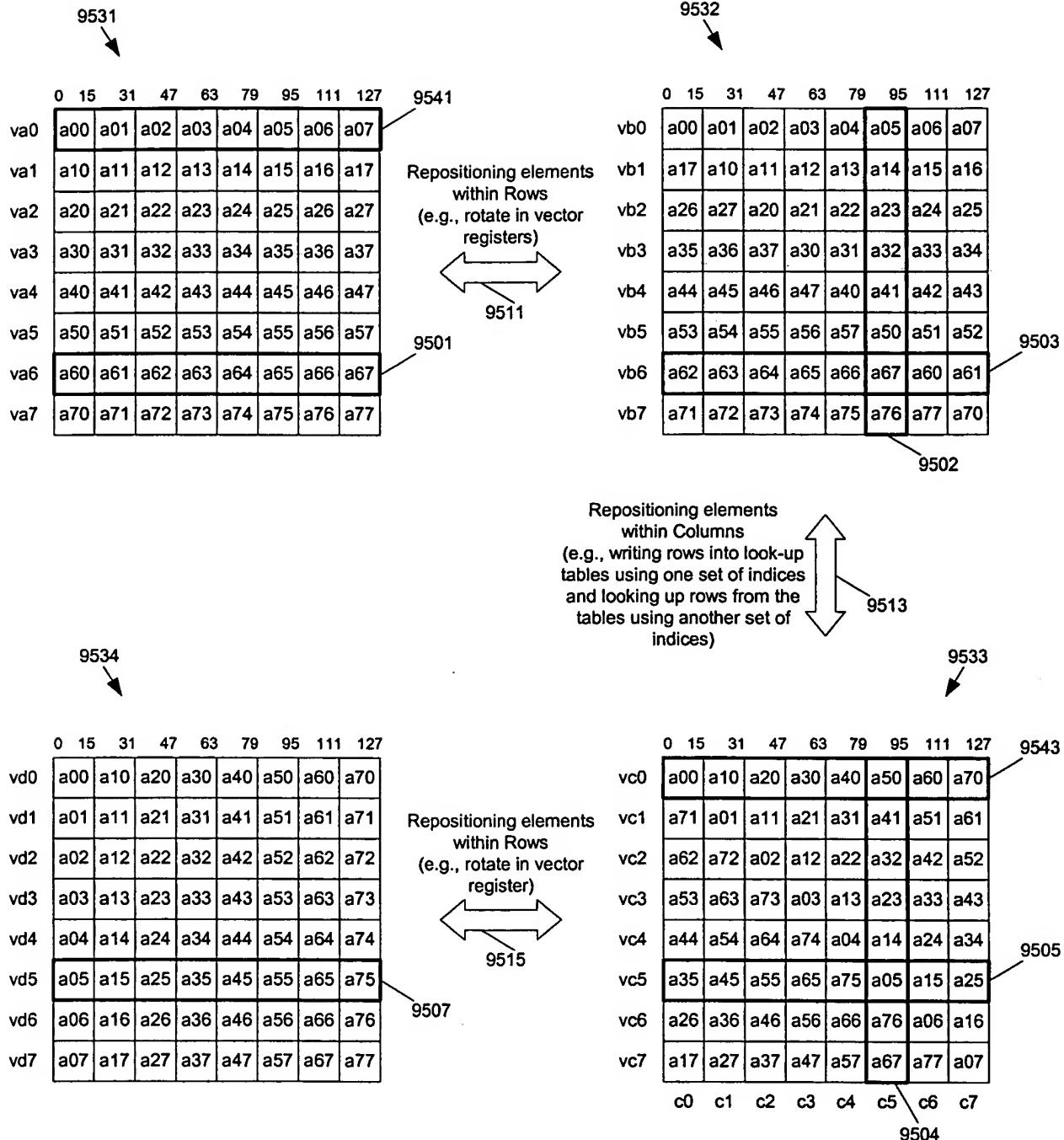


Fig. 75

9631

	0	7	15	23	31	39	47	55	63	71	79	87	95	103	111	119	127
vi0	0	0	1	1	2	2	3	3	4	4	5	5	6	6	7	7	
vi1	7	7	0	0	1	1	2	2	3	3	4	4	5	5	6	6	
vi2	6	6	7	7	0	0	1	1	2	2	3	3	4	4	5	5	
vi3	5	5	6	6	7	7	0	0	1	1	2	2	3	3	4	4	
vi4	4	4	5	5	6	6	7	7	0	0	1	1	2	2	3	3	
vi5	3	3	4	4	5	5	6	6	7	7	0	0	1	1	2	2	
vi6	2	2	3	3	4	4	5	5	6	6	7	7	0	0	1	1	
vi7	1	1	2	2	3	3	4	4	5	5	6	6	7	7	0	0	
	T0	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14	T15	

9633

	0	7	15	23	31	39	47	55	63	71	79	87	95	103	111	119	127
vj0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
vj1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
vj2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	
vj3	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3	
vj4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	
vj5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	
vj6	6	6	6	6	6	6	6	6	6	6	6	6	6	6	6	6	
vj7	7	7	7	7	7	7	7	7	7	7	7	7	7	7	7	7	
	T0	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14	T15	

Fig. 76

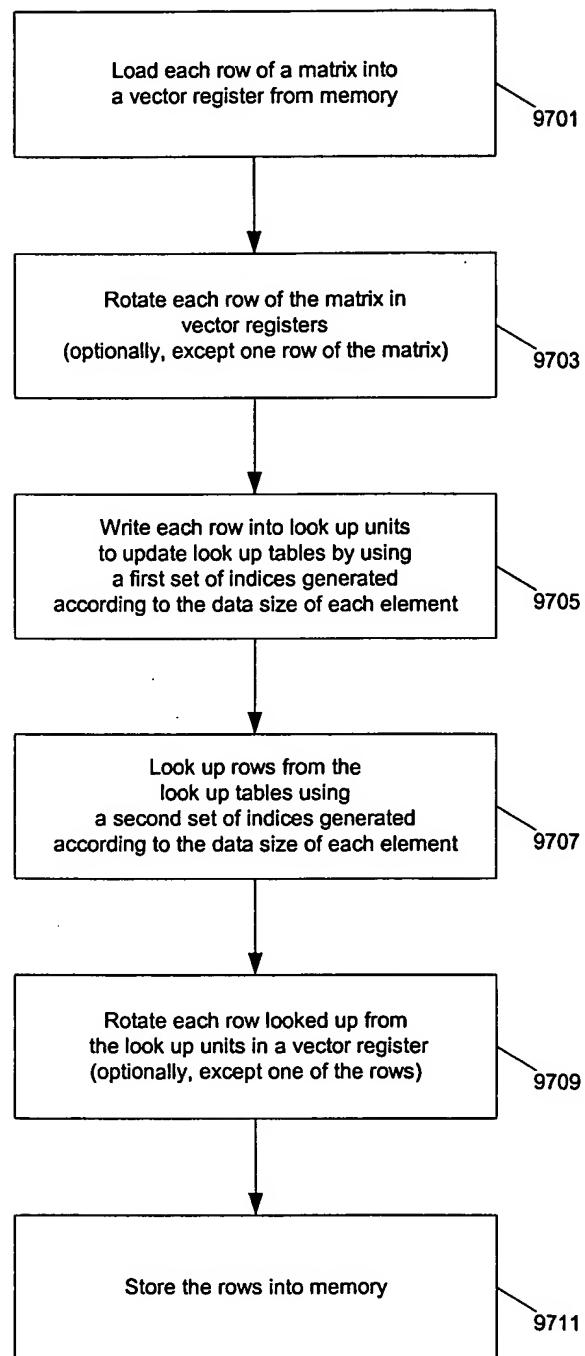


Fig. 77

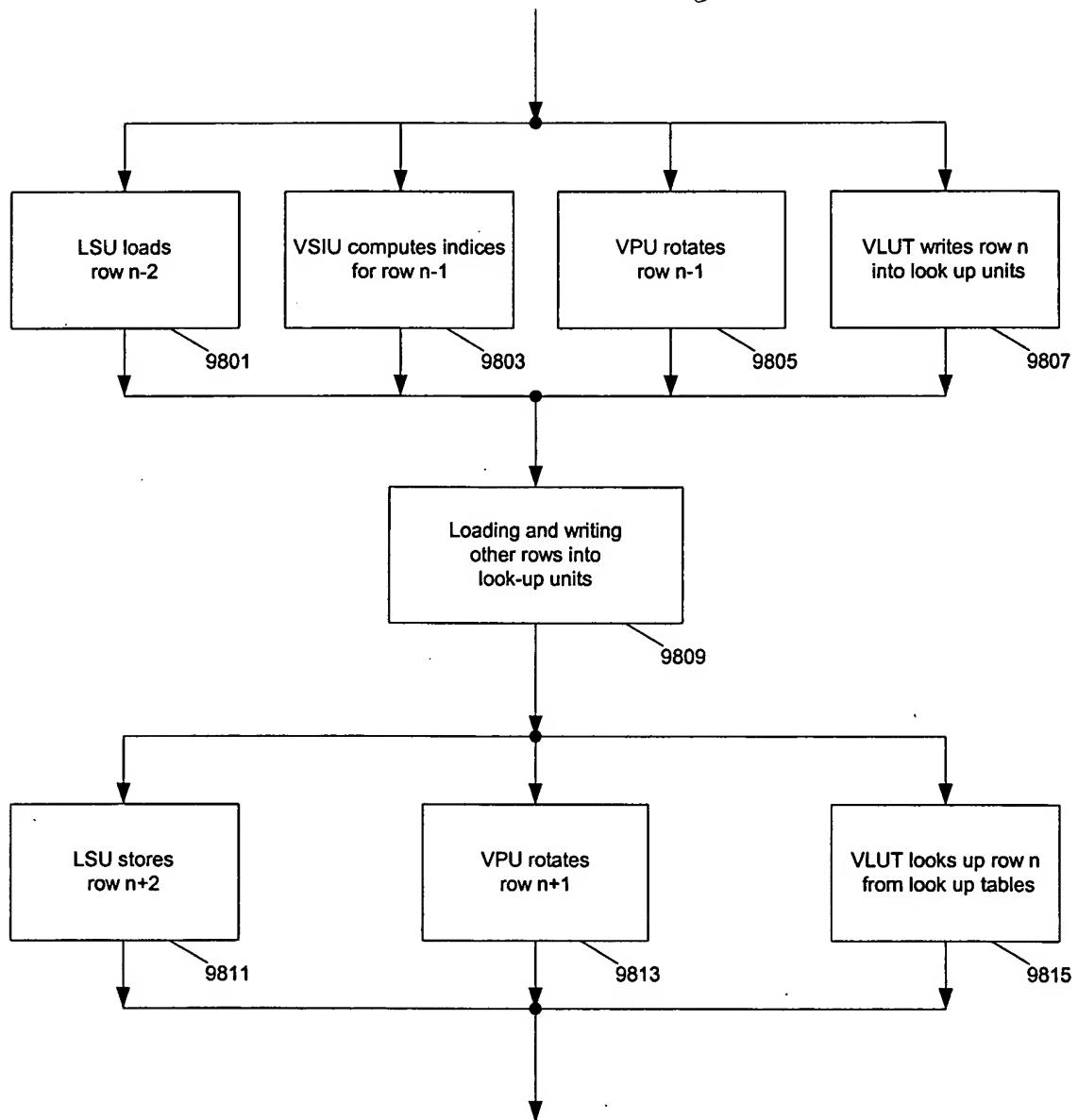


Fig. 78

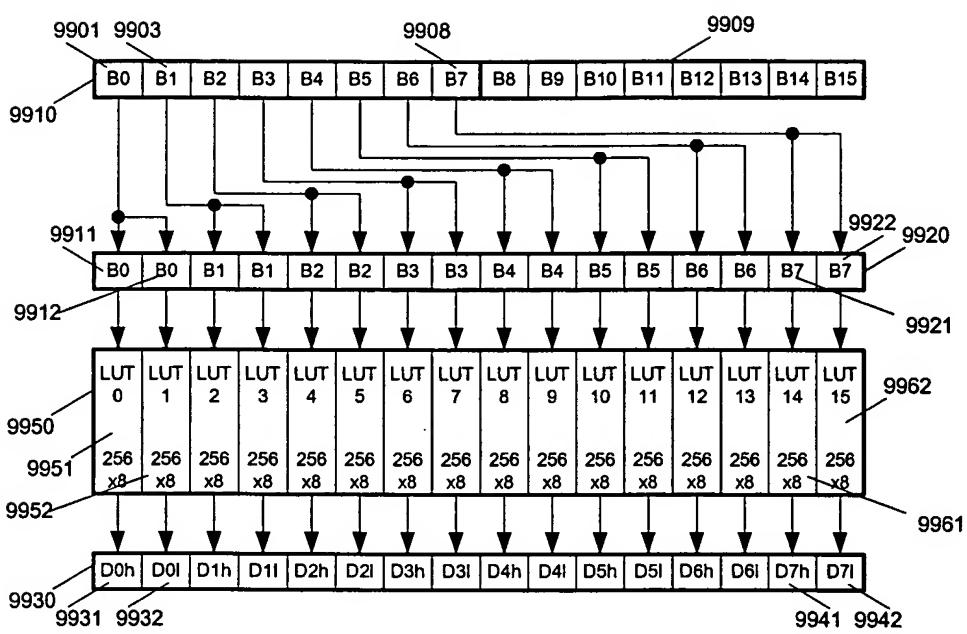


Fig. 79

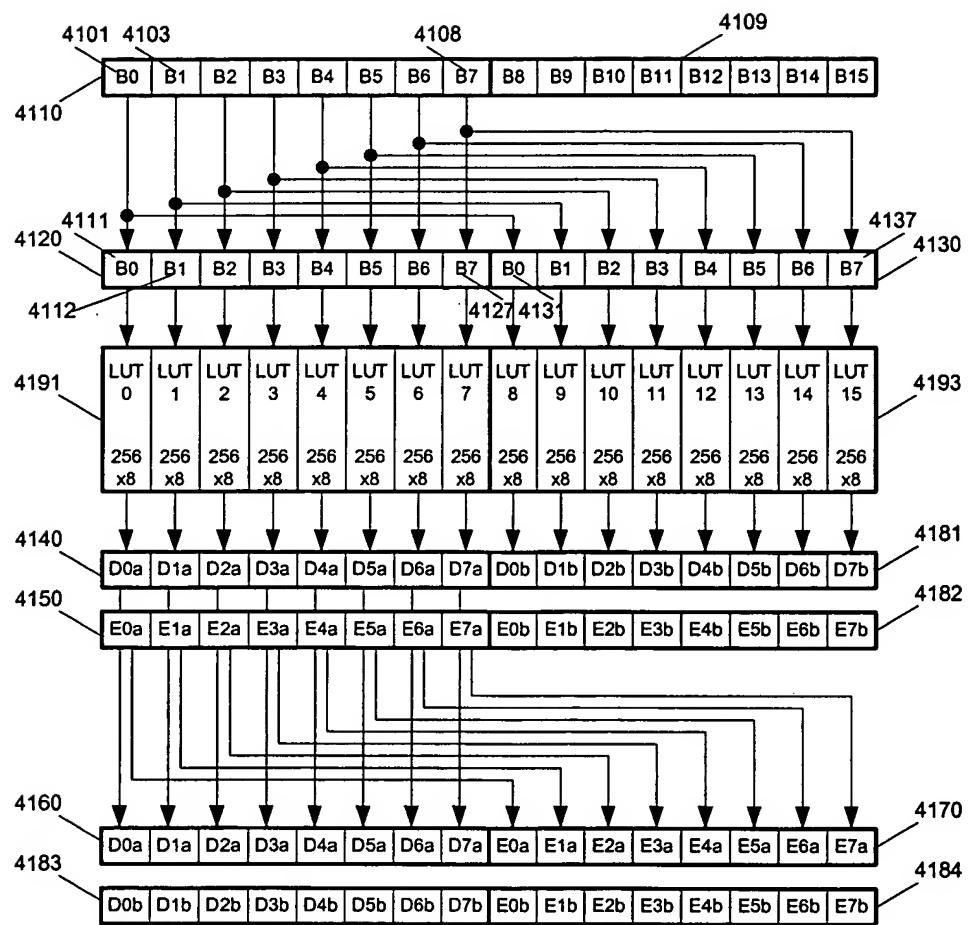


Fig. 80

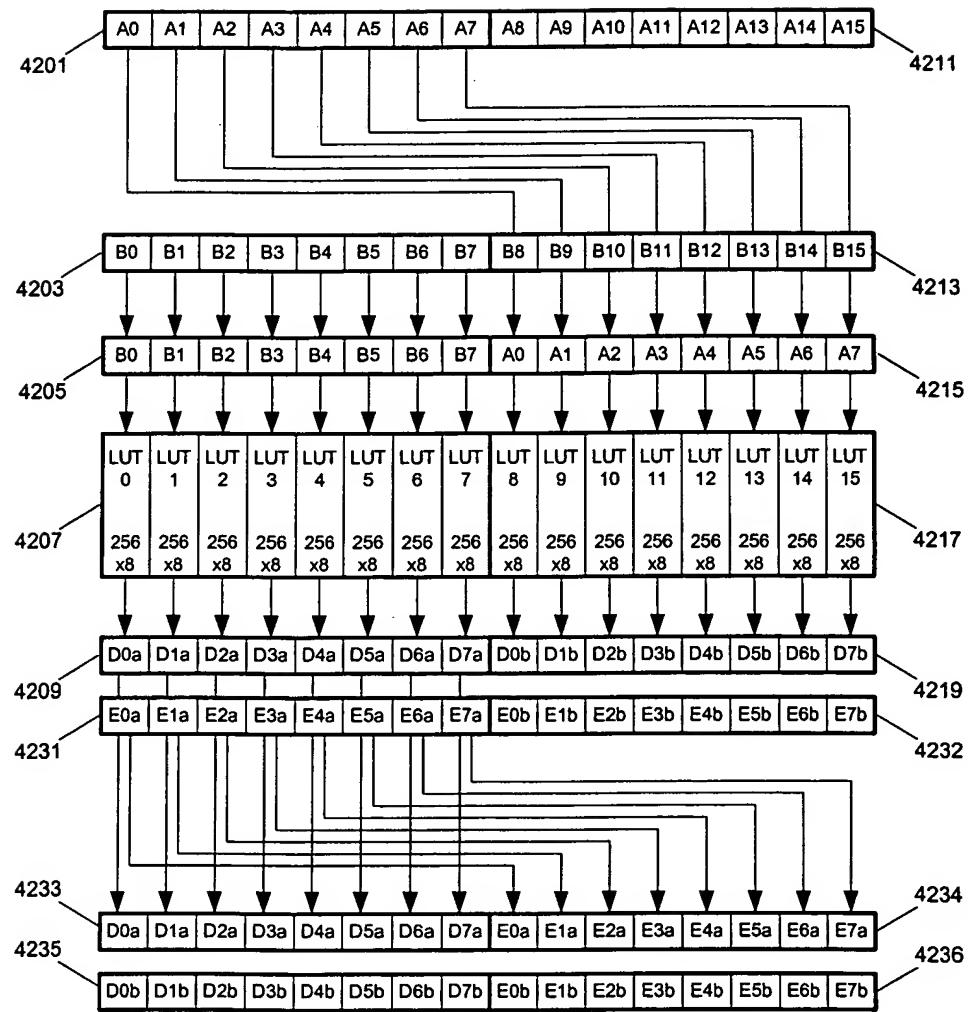


Fig. 81

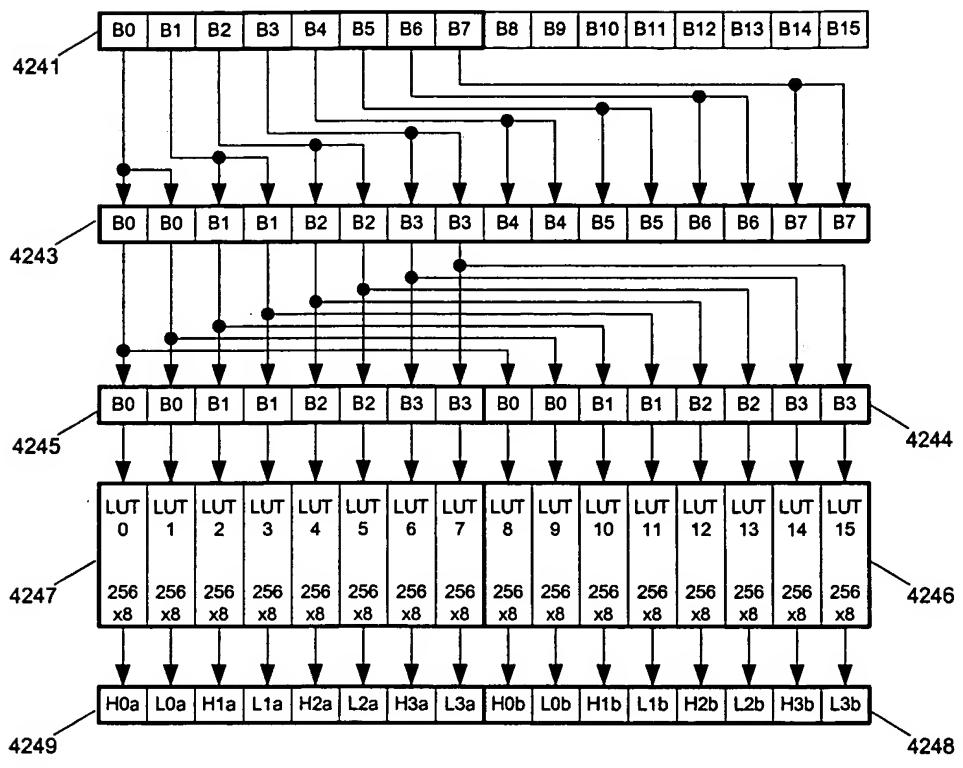


Fig. 82

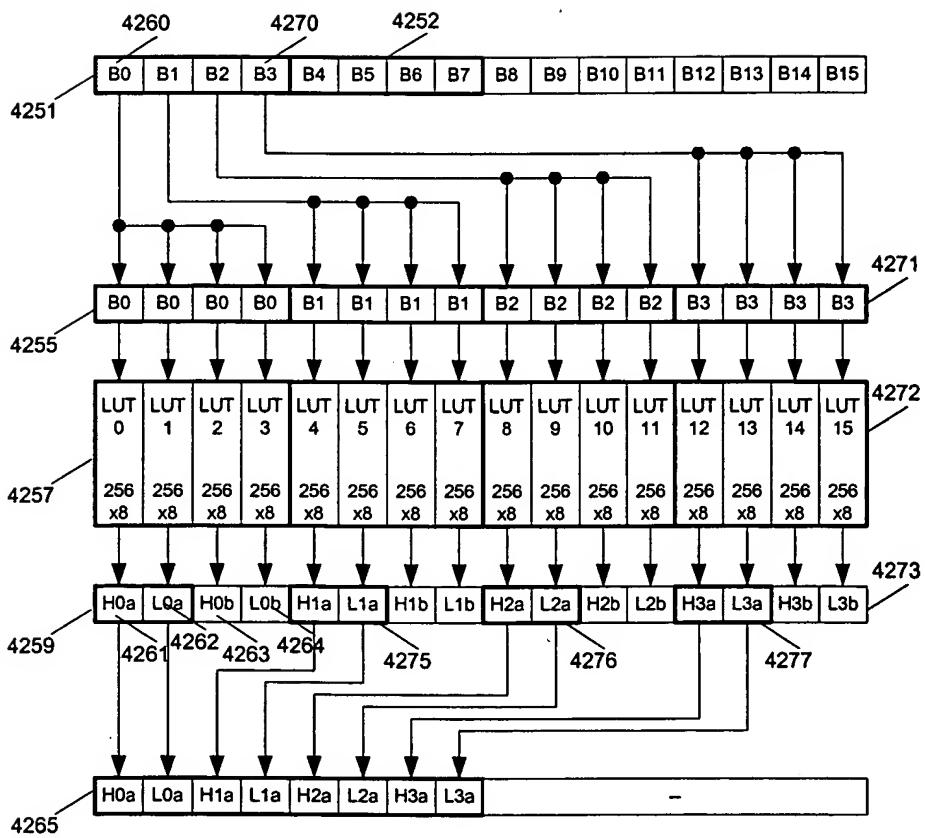


Fig. 83

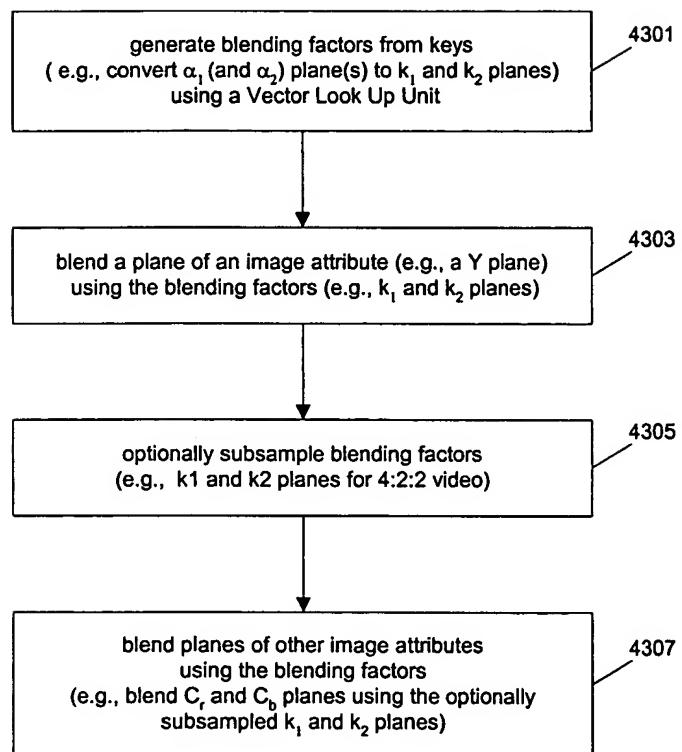


Fig. 84

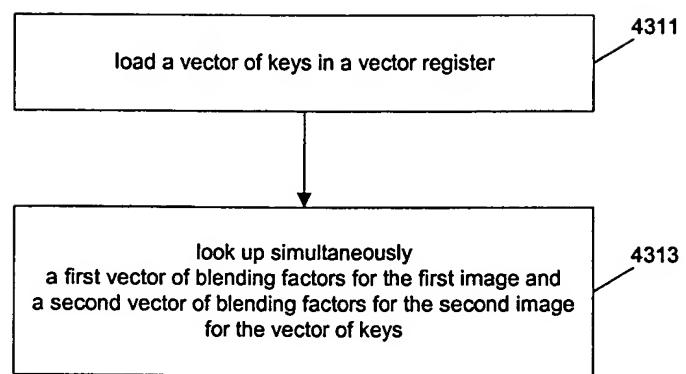


Fig. 85

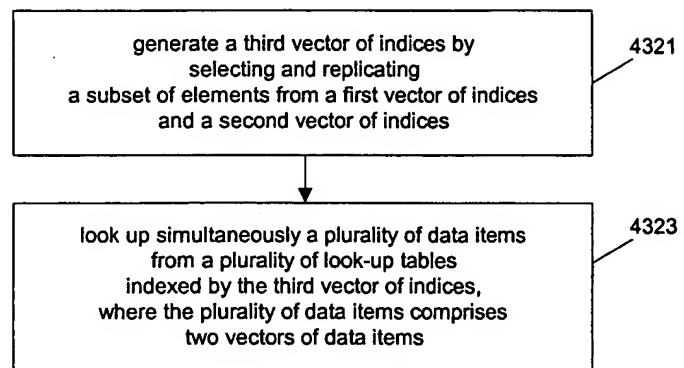


Fig. 86

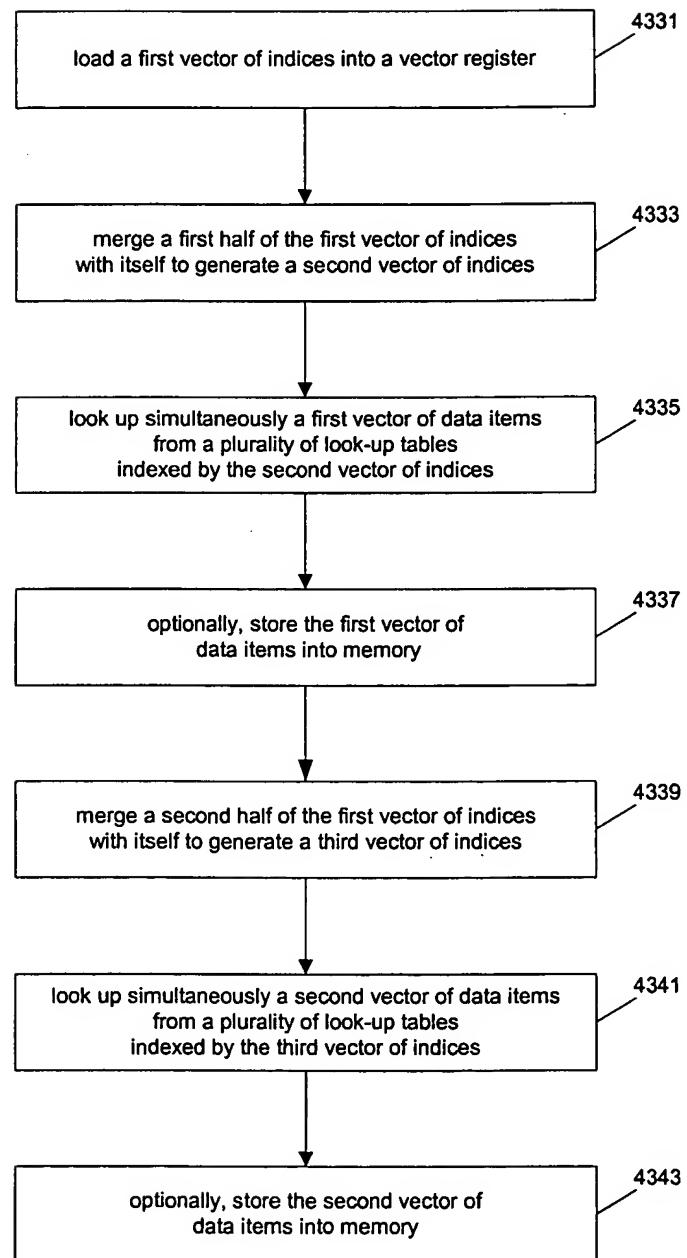


Fig. 87

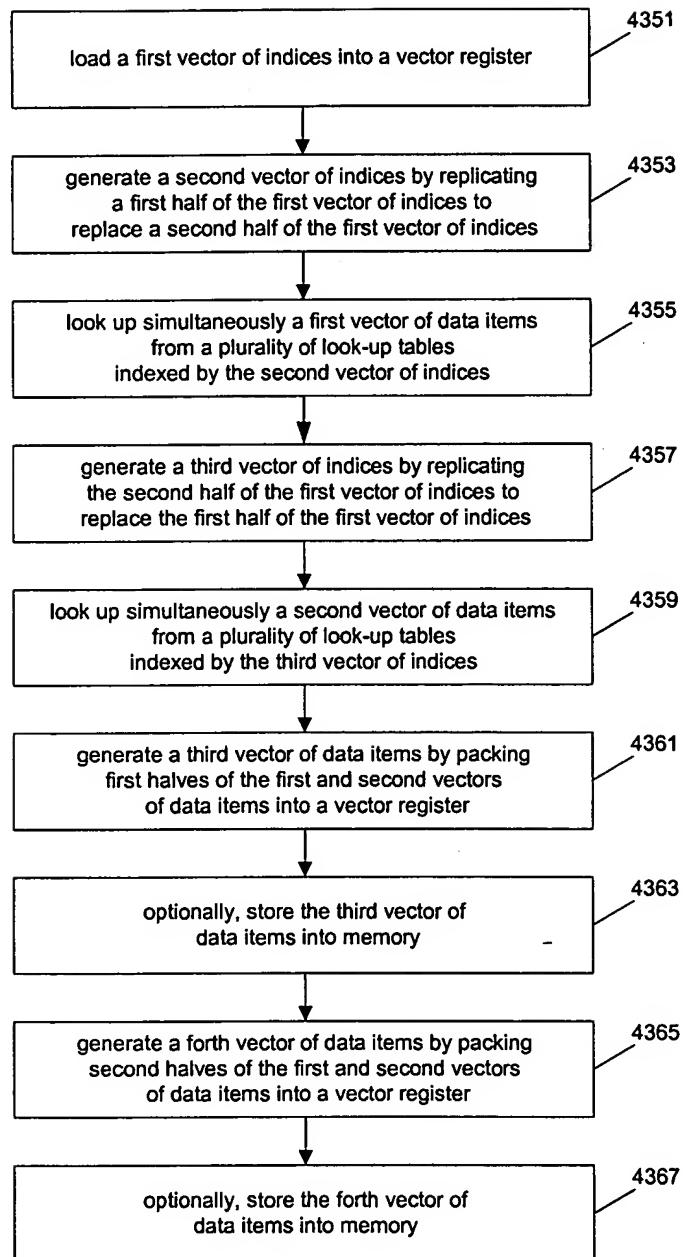


Fig. 88

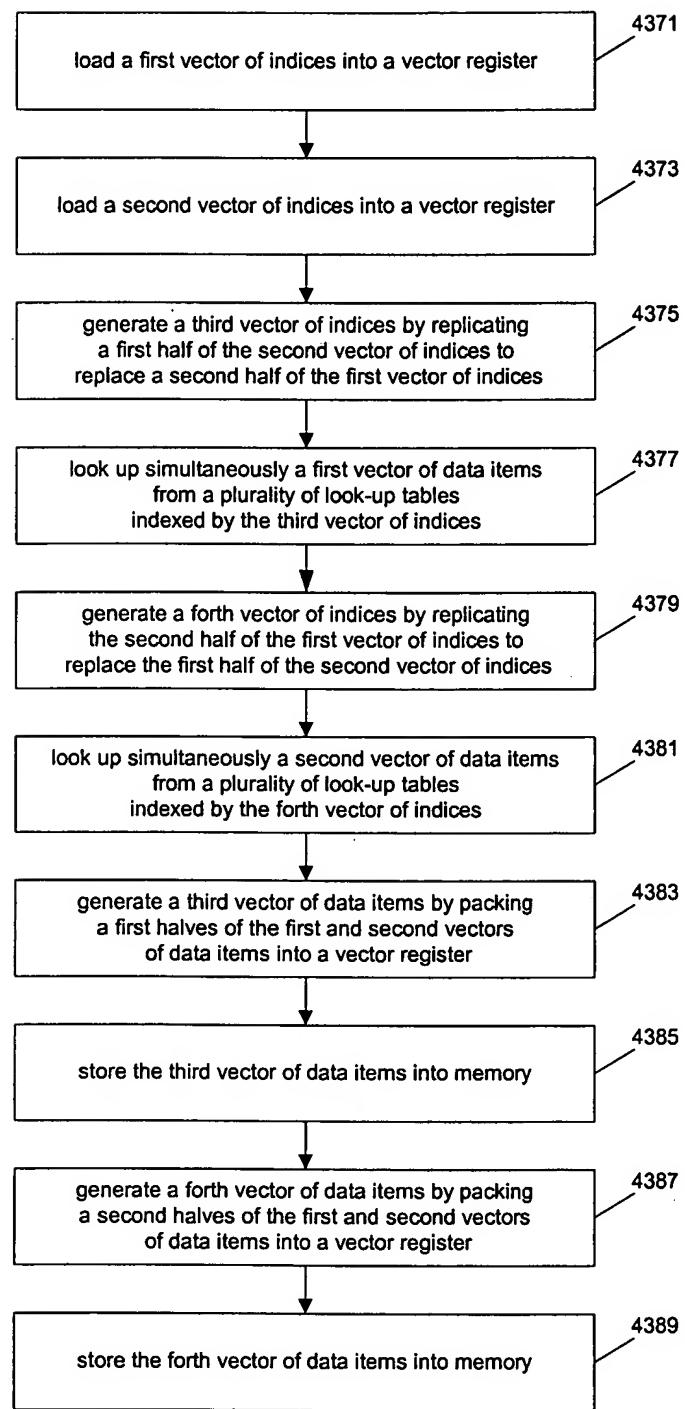


Fig. 89

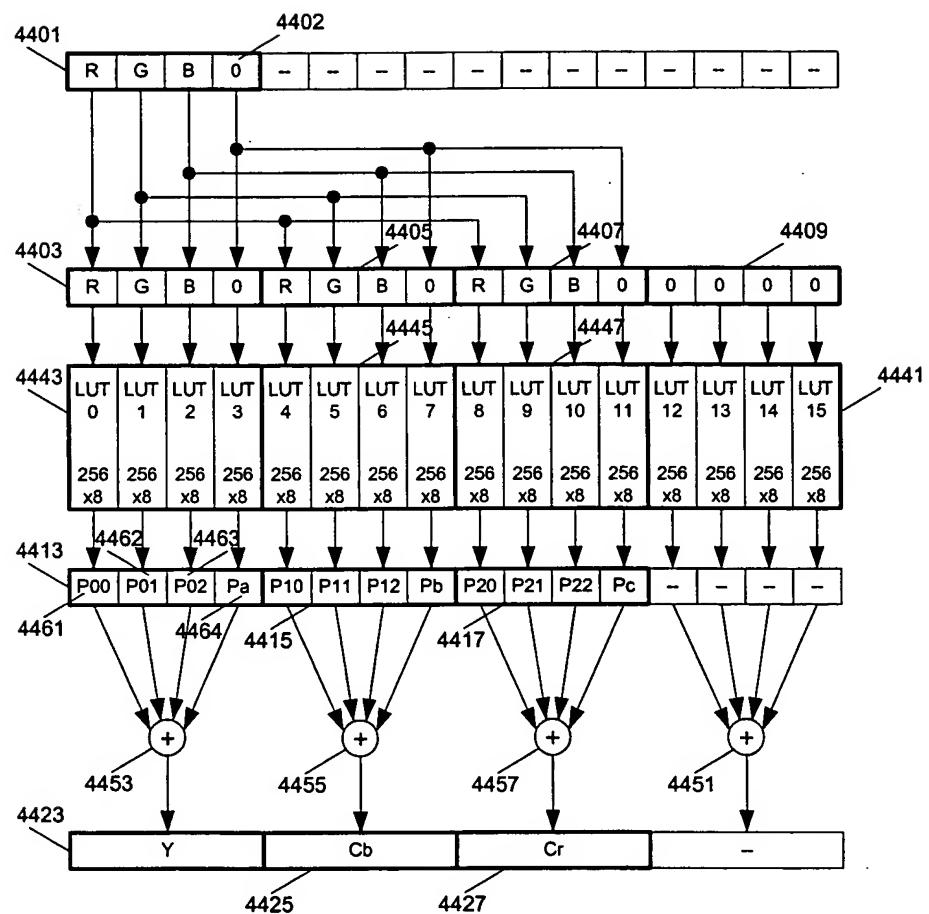


Fig. 90

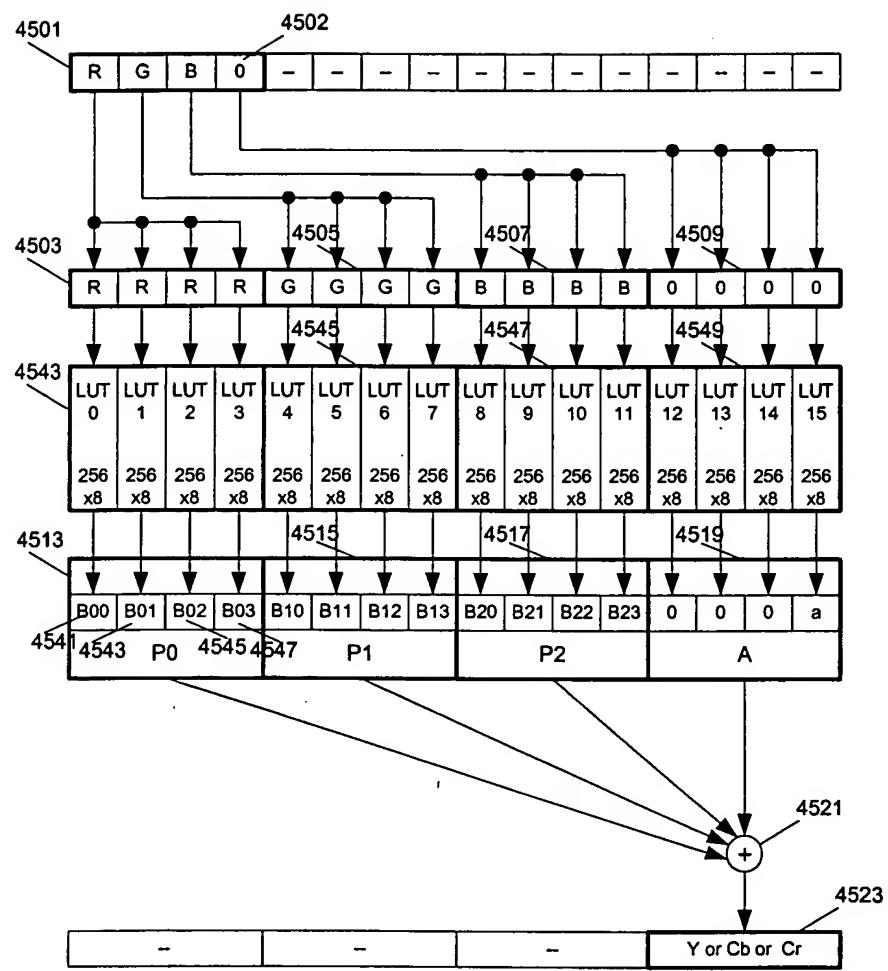


Fig. 91

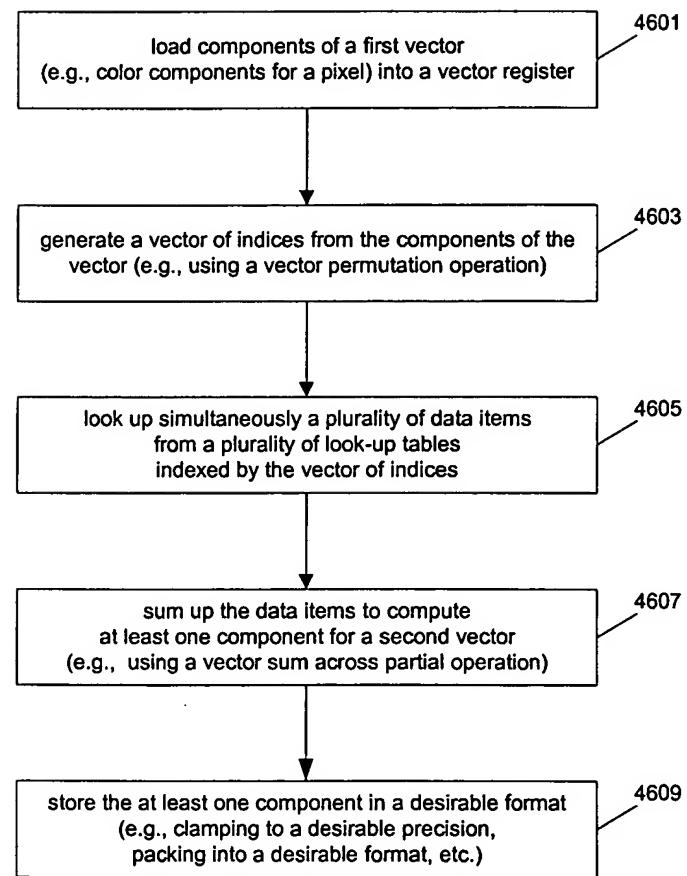


Fig. 92

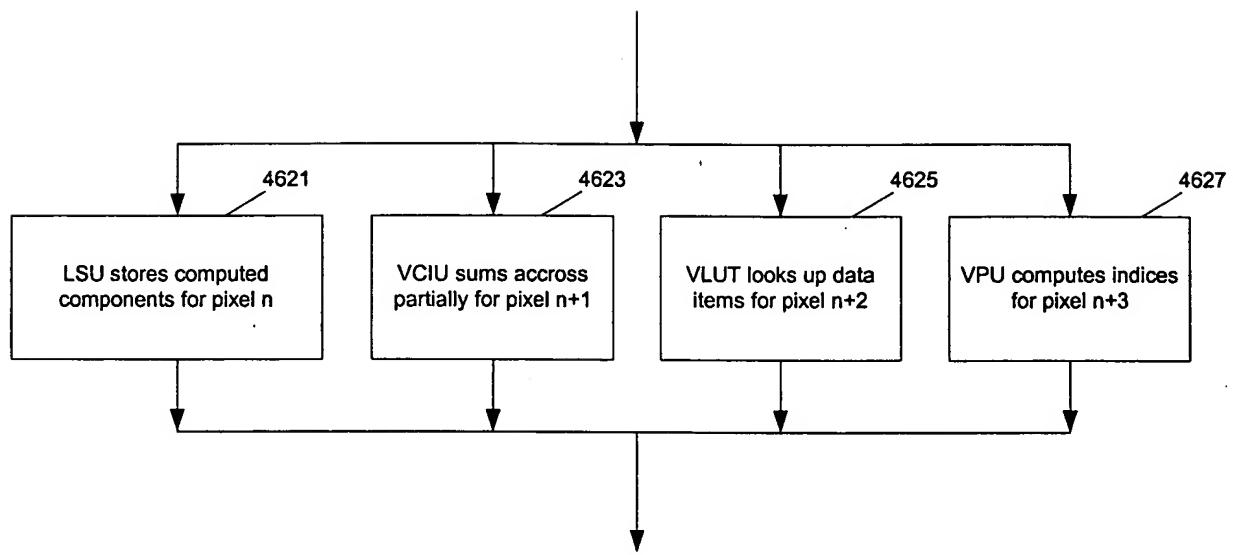


Fig. 93

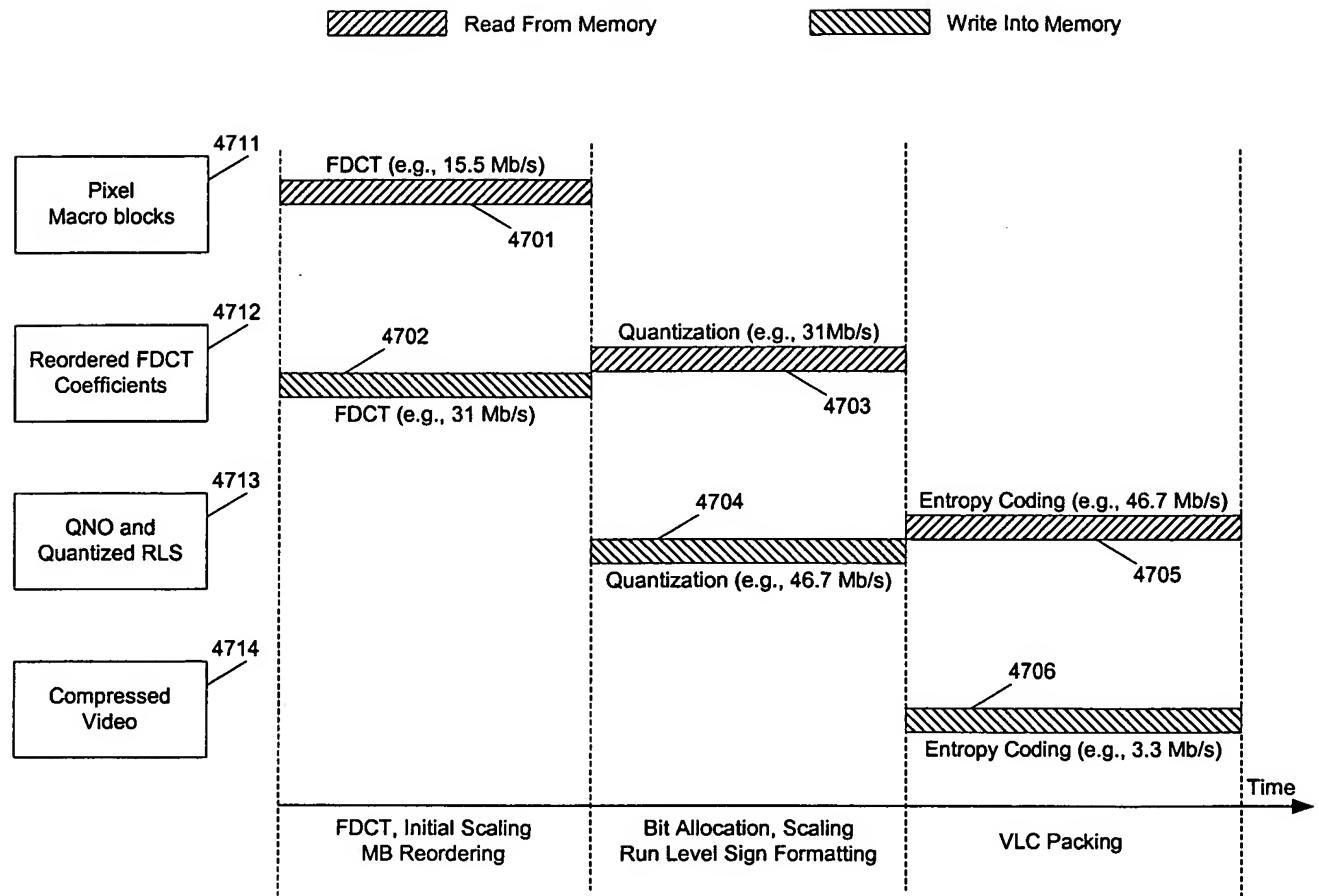


Fig. 94

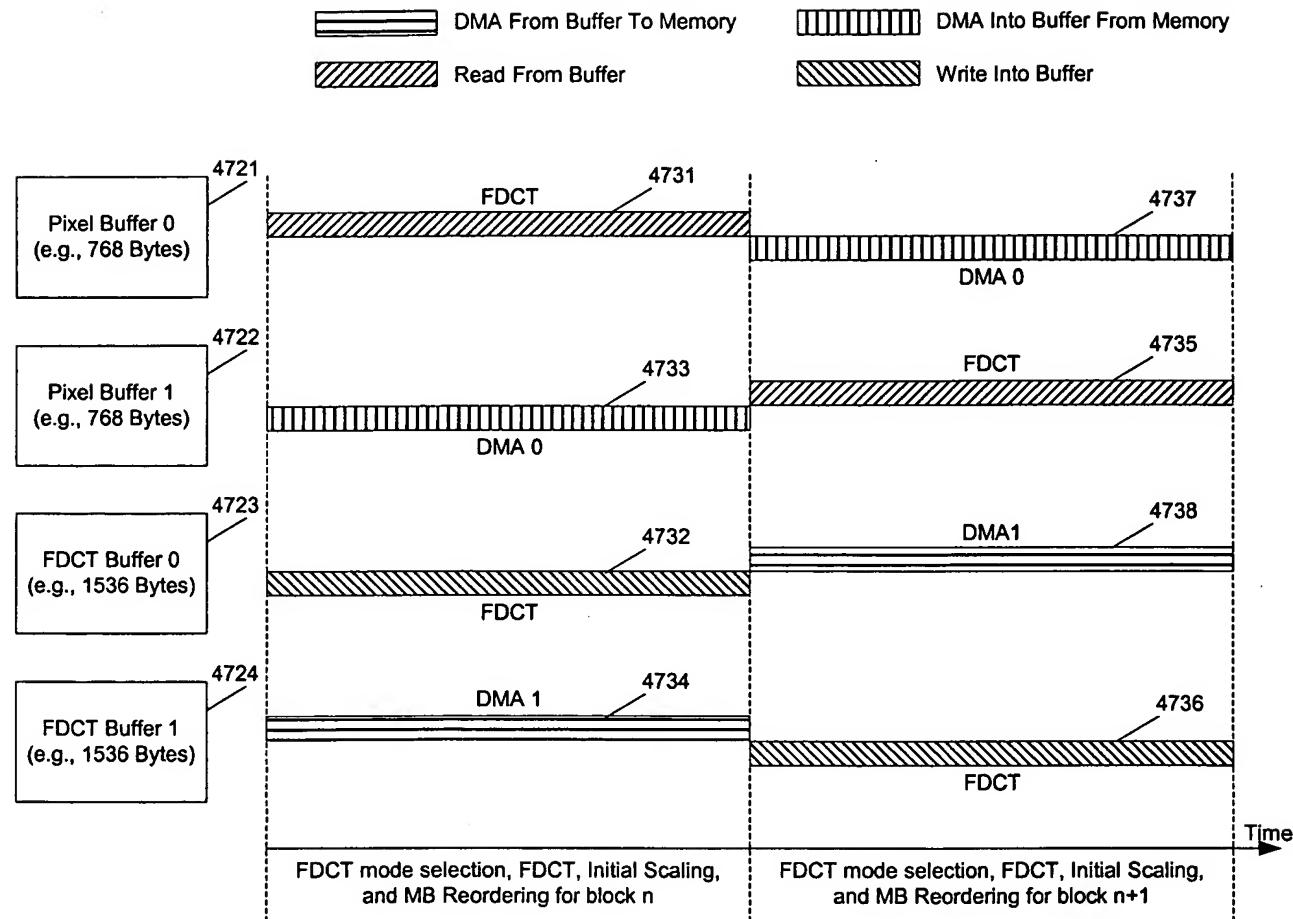


Fig. 95

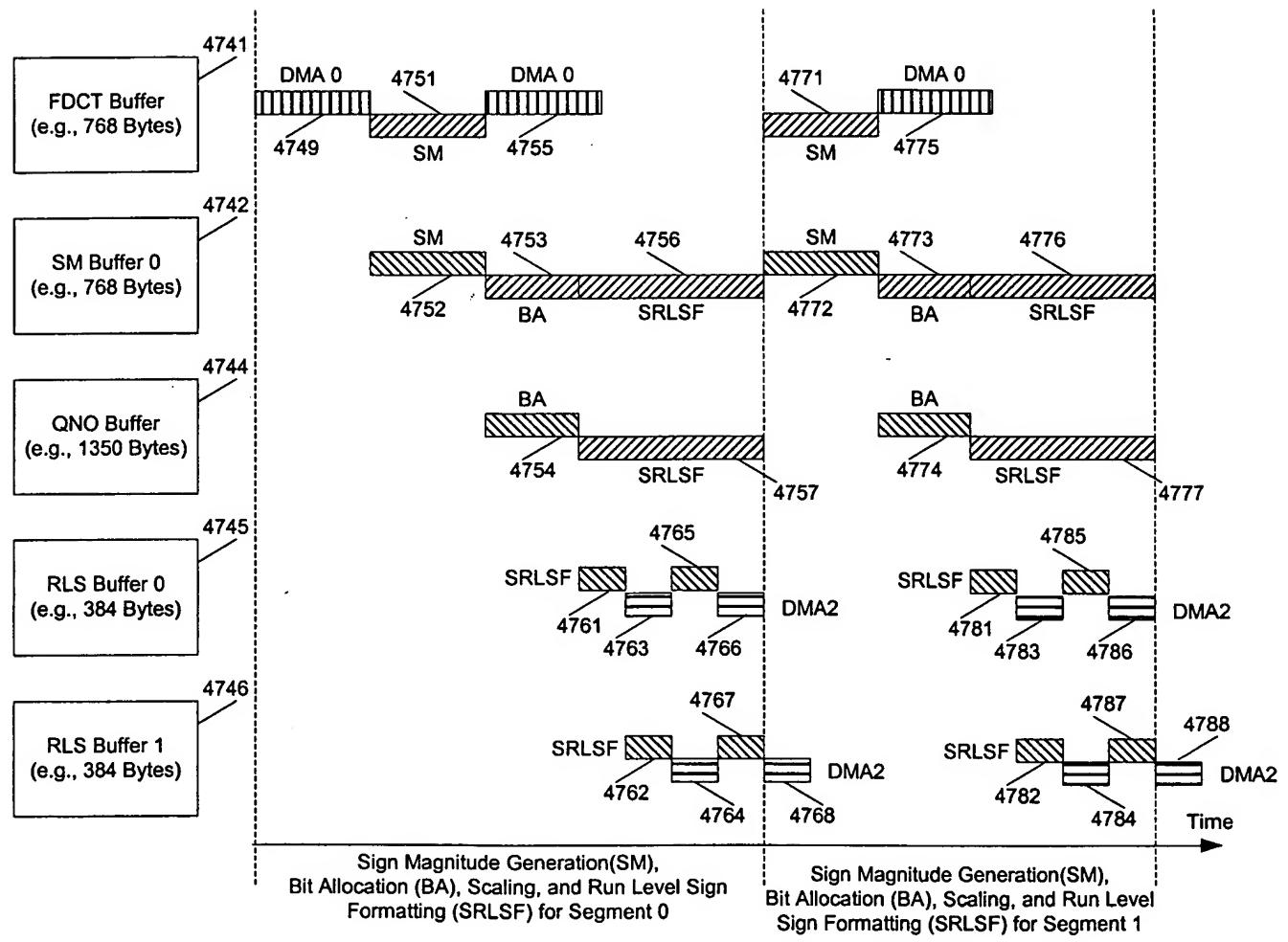
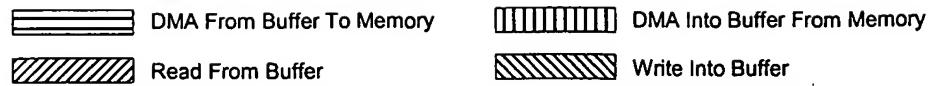
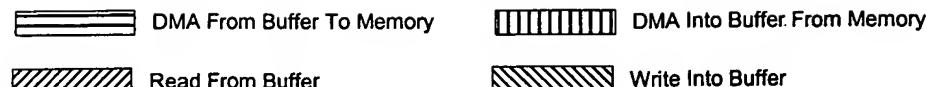


Fig. 96



4801  
4802  
4803  
4804  
4805  
4806  
4807

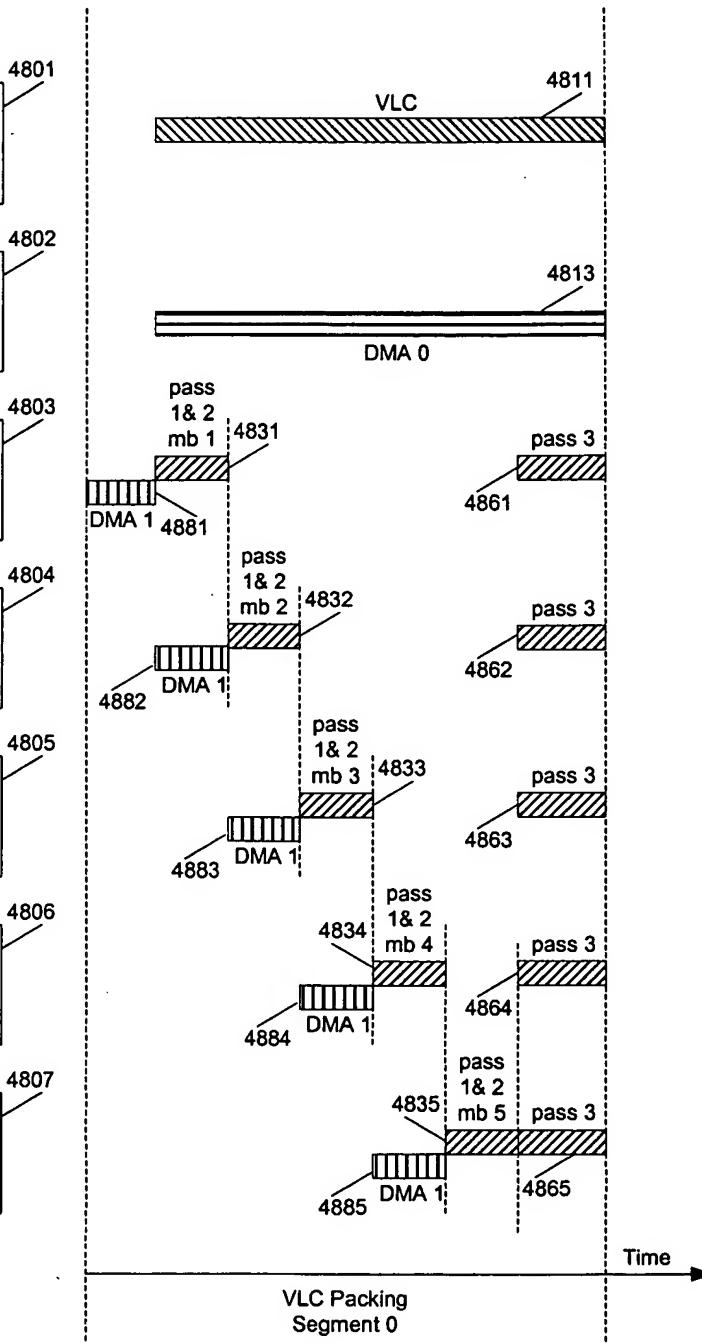
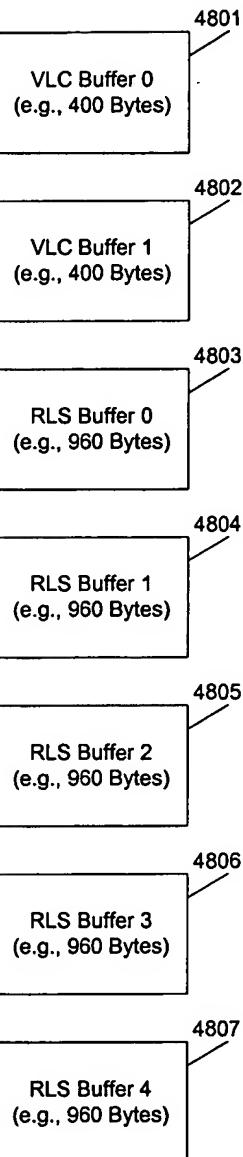


Fig. 97